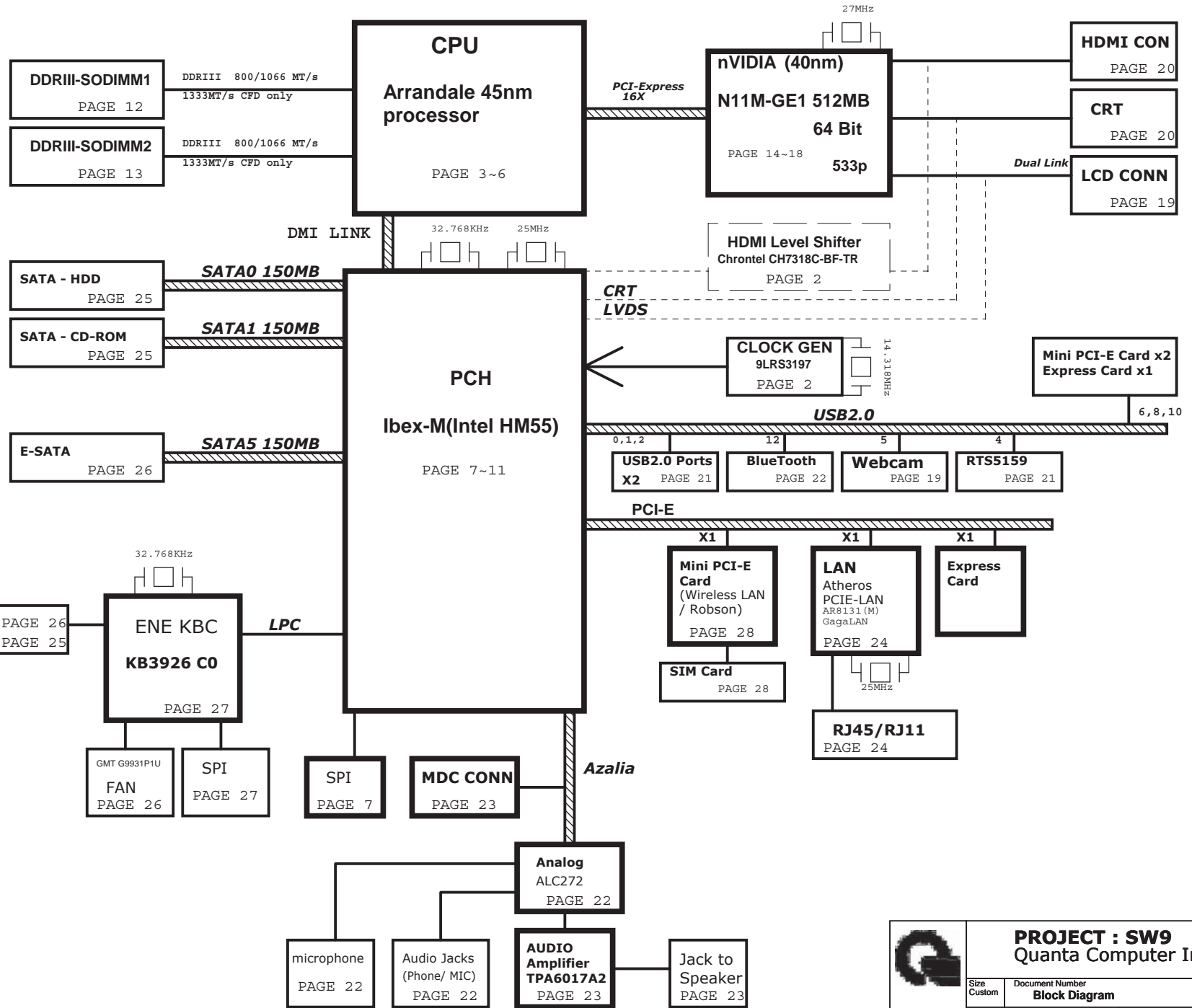


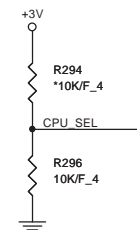
PCB STACK UP
6L Dis. & UMA

SW9 (14") BLOCK DIAGRAM

01

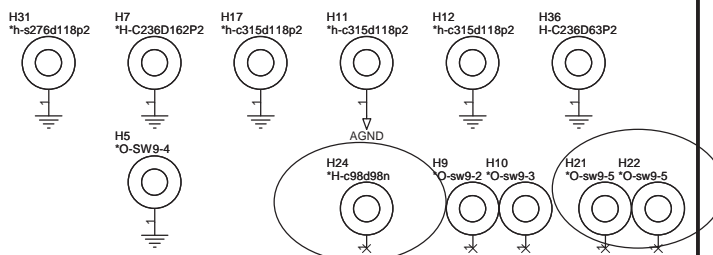
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



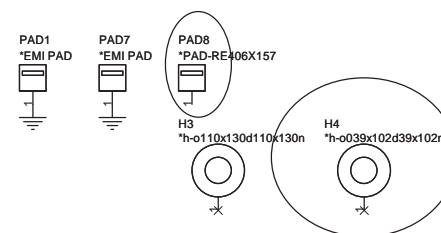
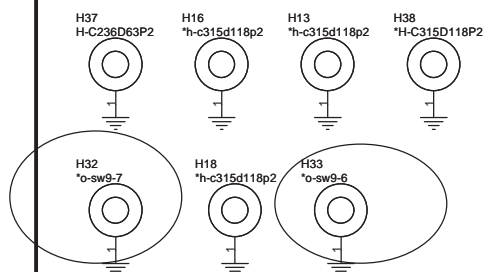


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

PAD and HOLE



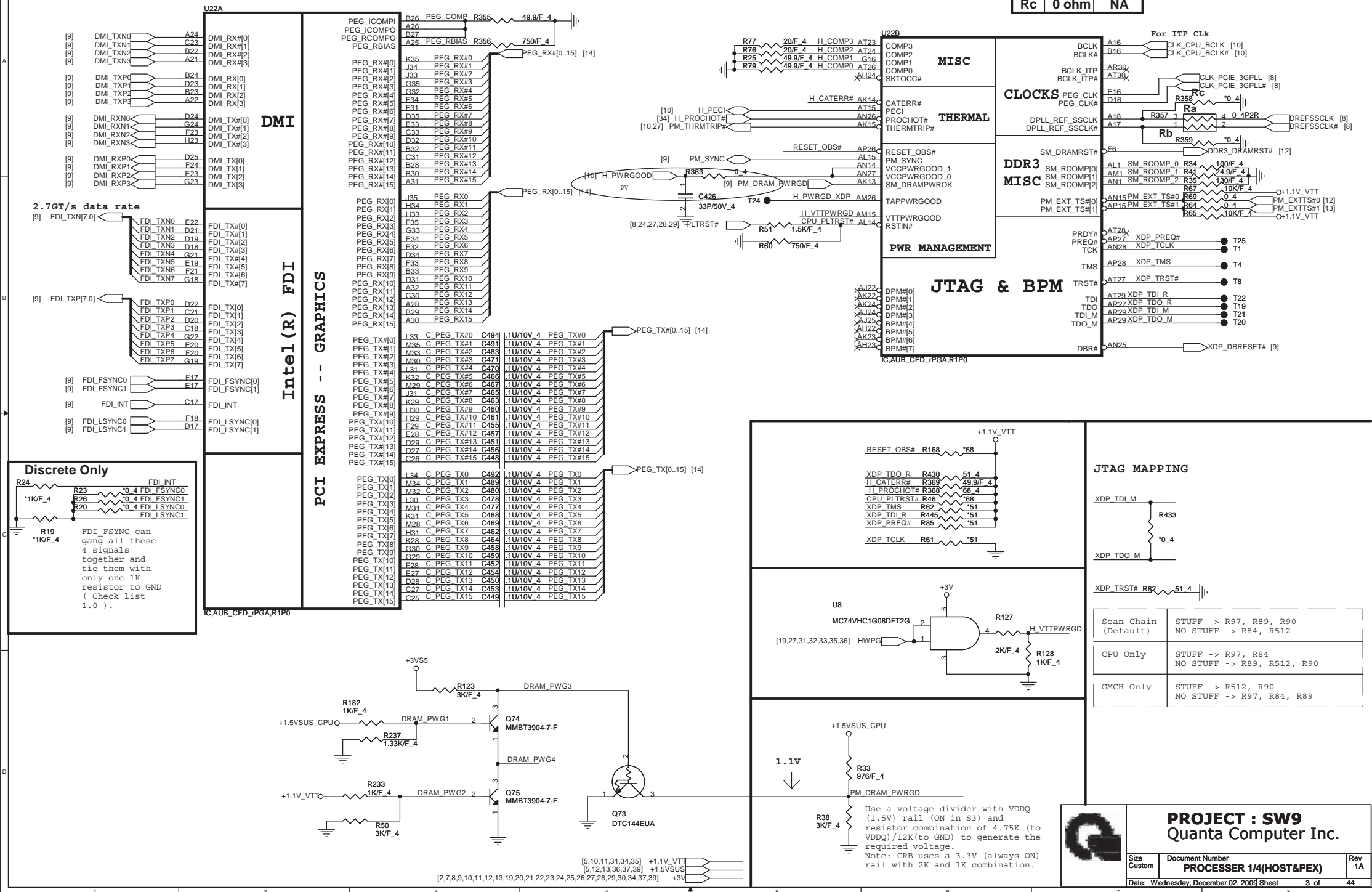
MINI CARD Hole.



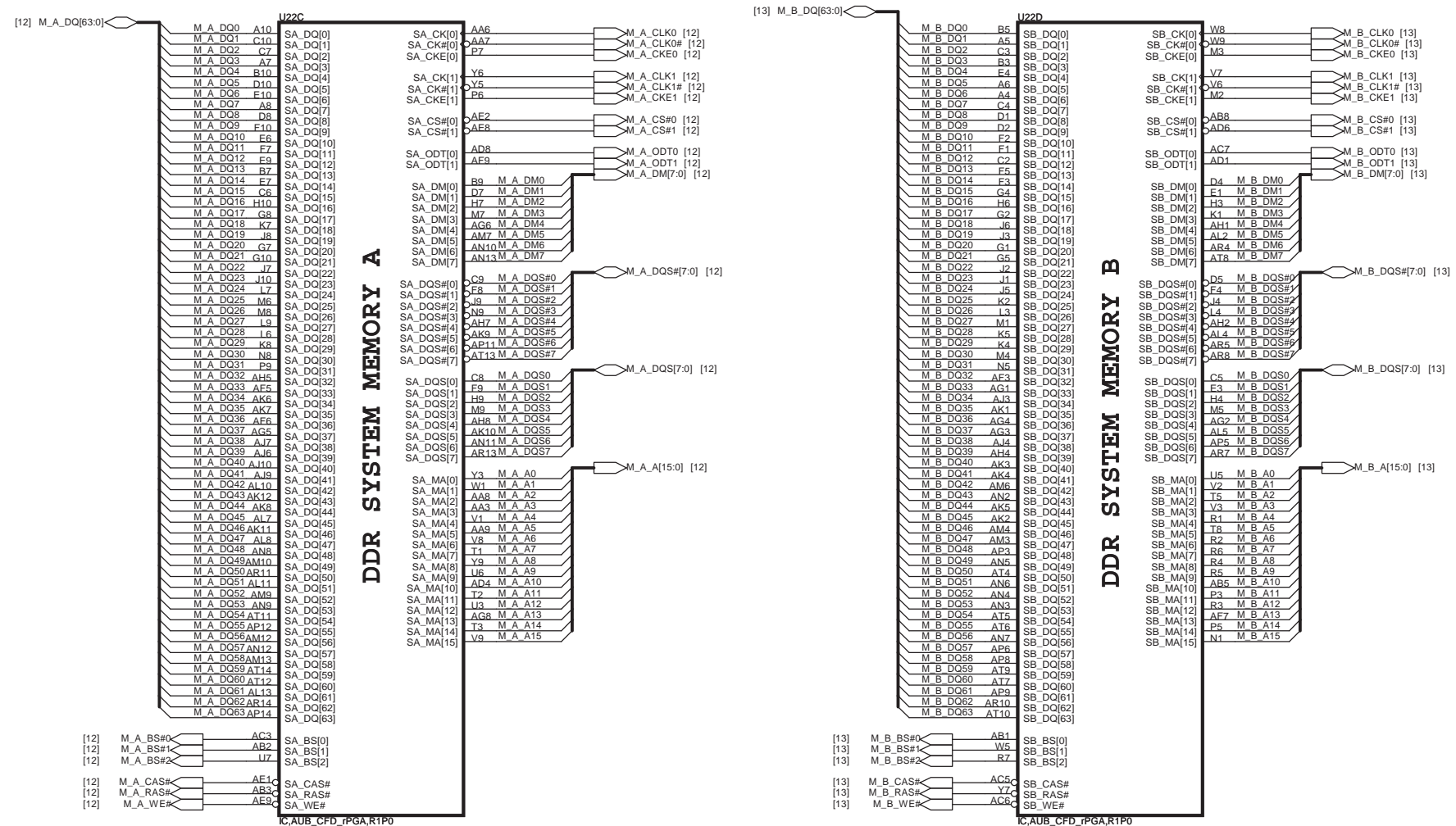
PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number CLOCK & Screw Holes	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 2 of 44		

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

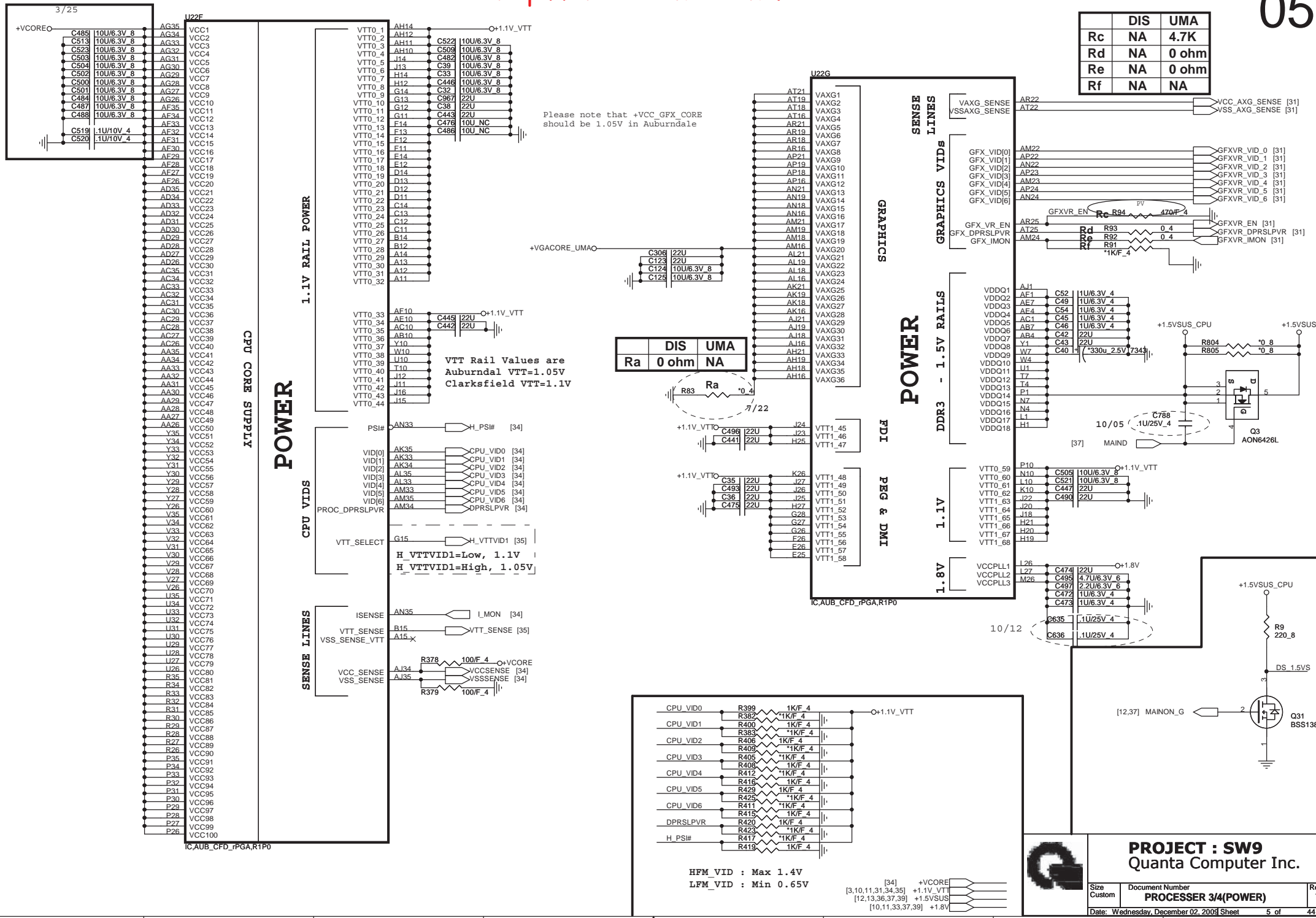


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



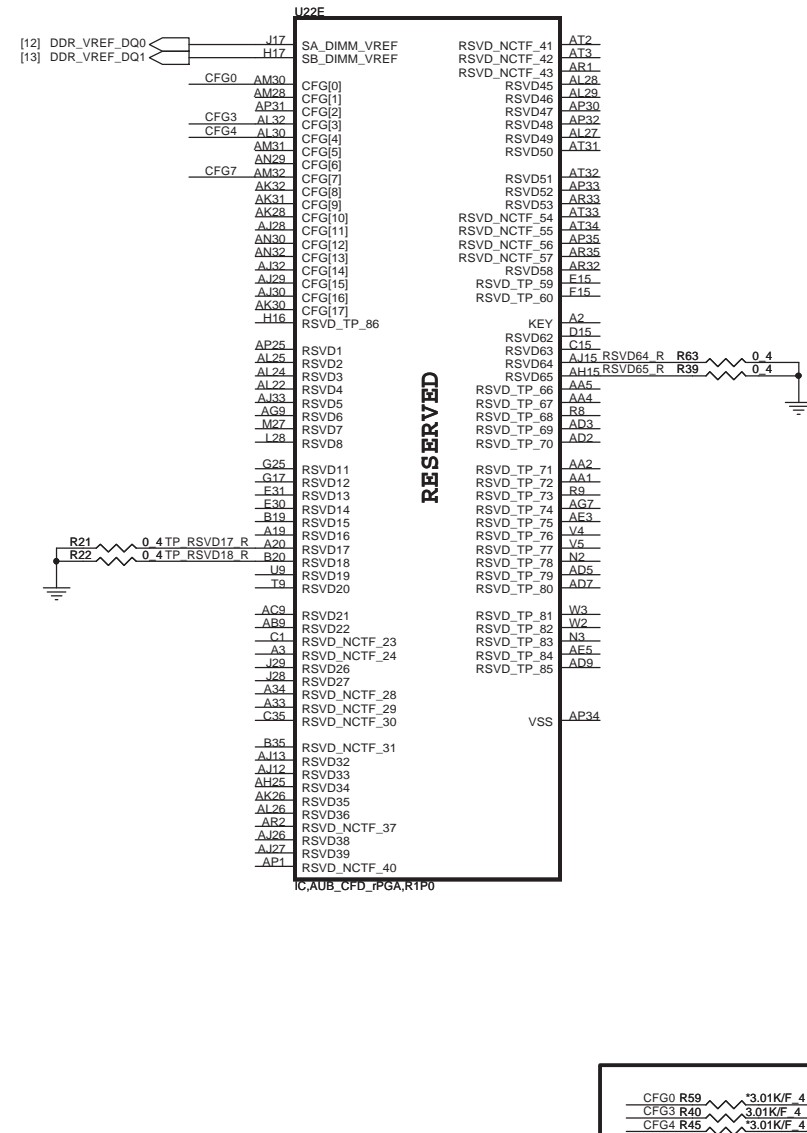
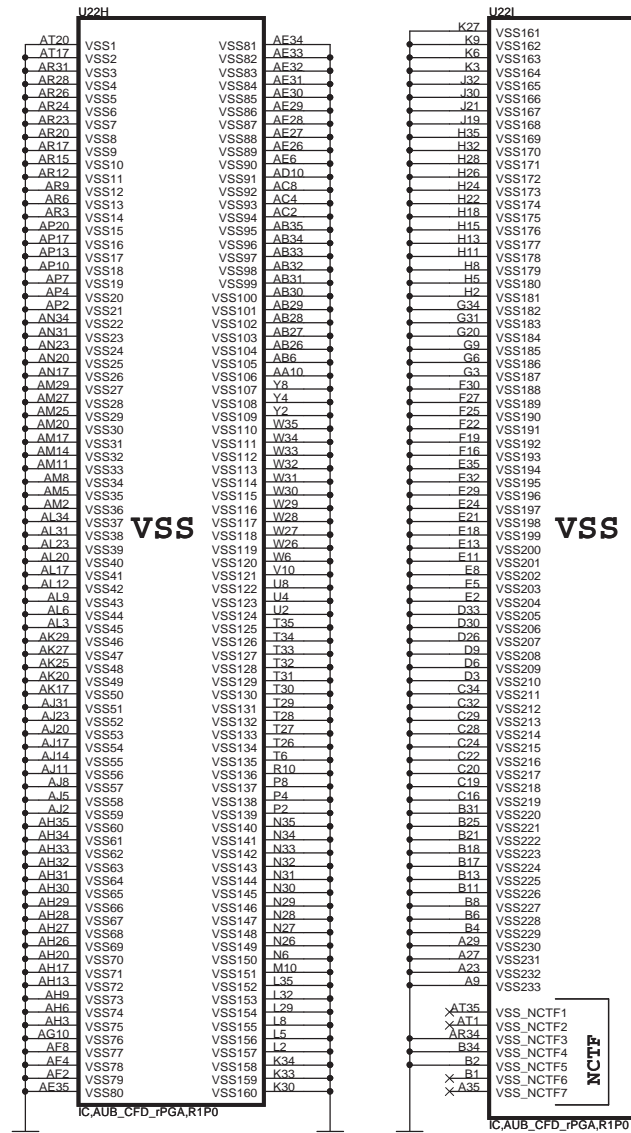
PROJECT : SW9
Quanta Computer Inc.

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA



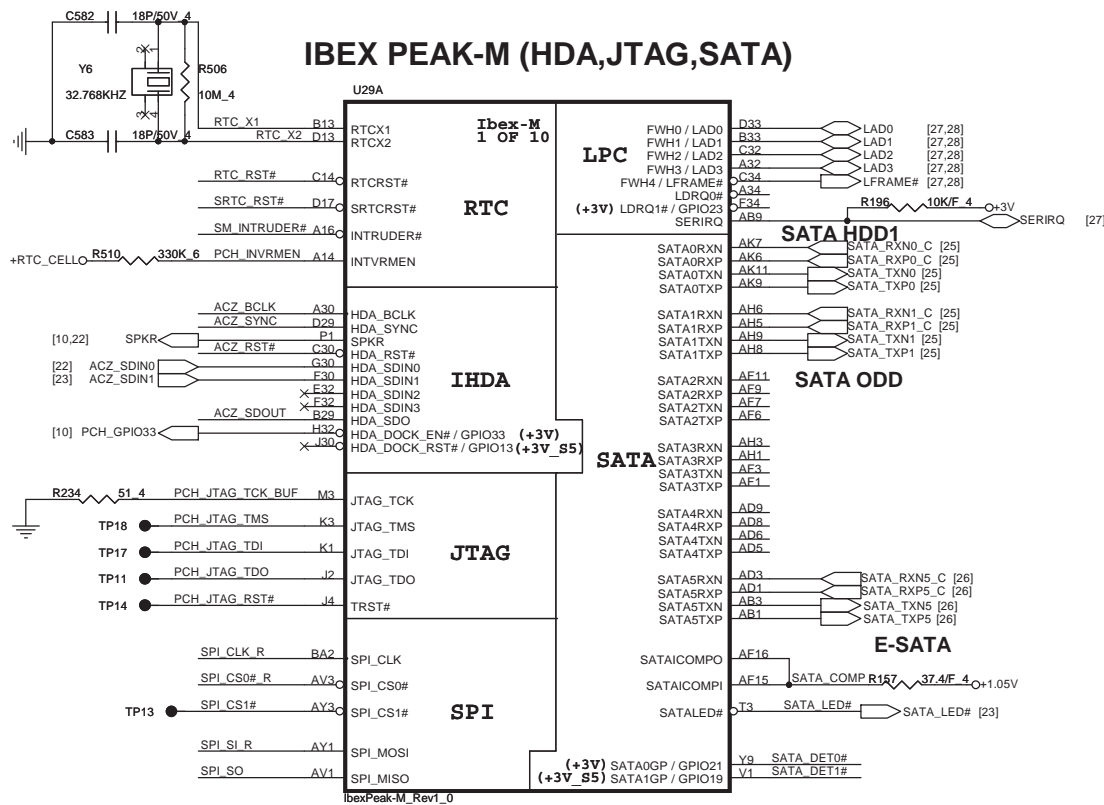
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

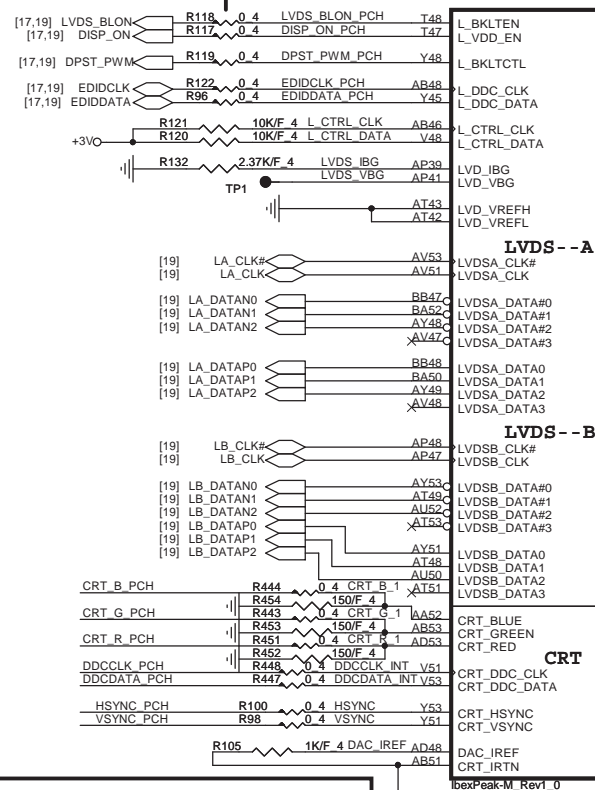


INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

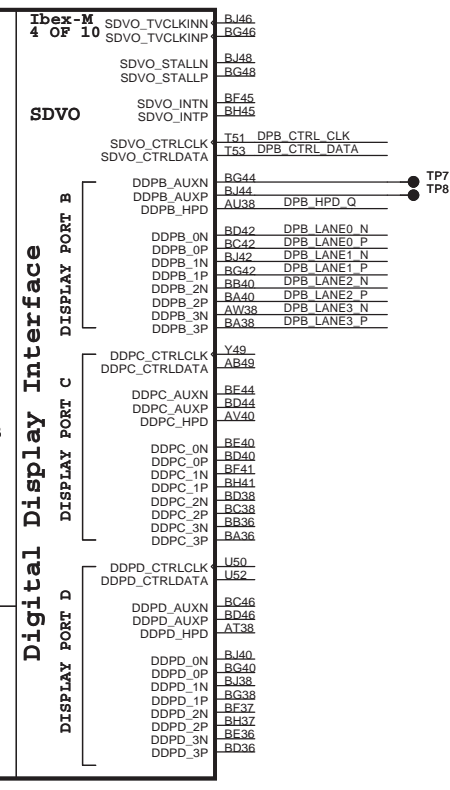
IBEX PEAK-M (HDA,JTAG,SATA)



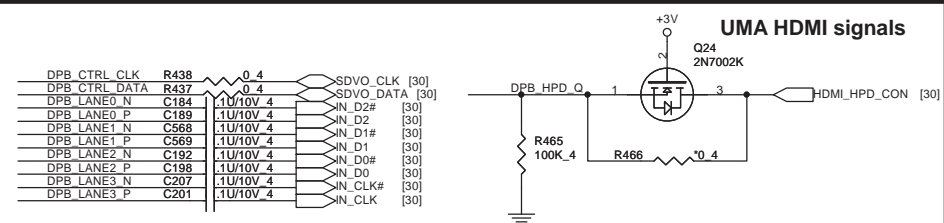
UMA LVDS & CRT signals



IBEX PEAK-M (LVDS,DDI)

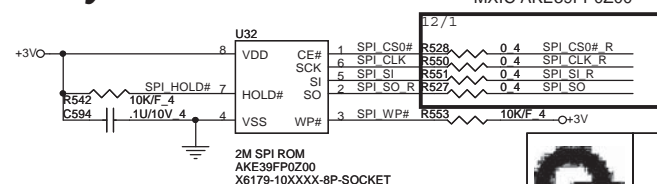


UMA HDMI signals

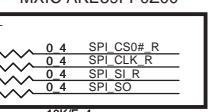


UMA only

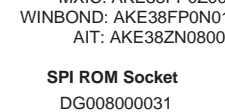
2M byte SPI ROM for ME



4M byte SPI ROM for ME



2M byte SPI ROM for ME

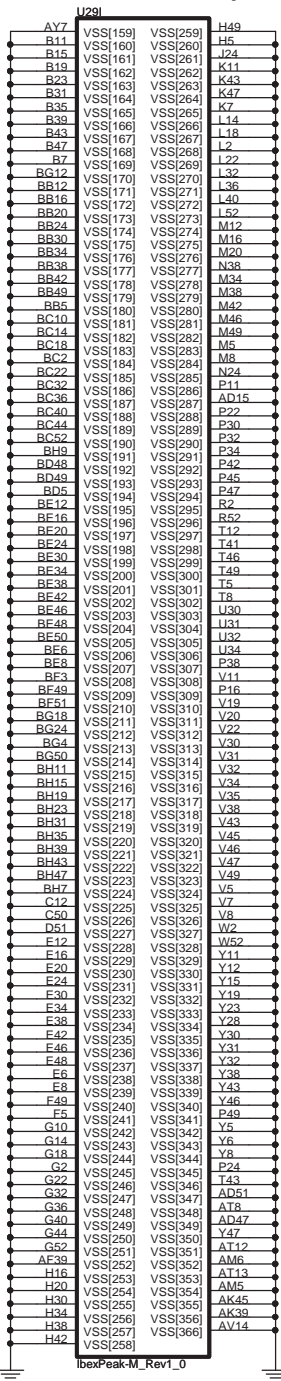


PROJECT : SW9

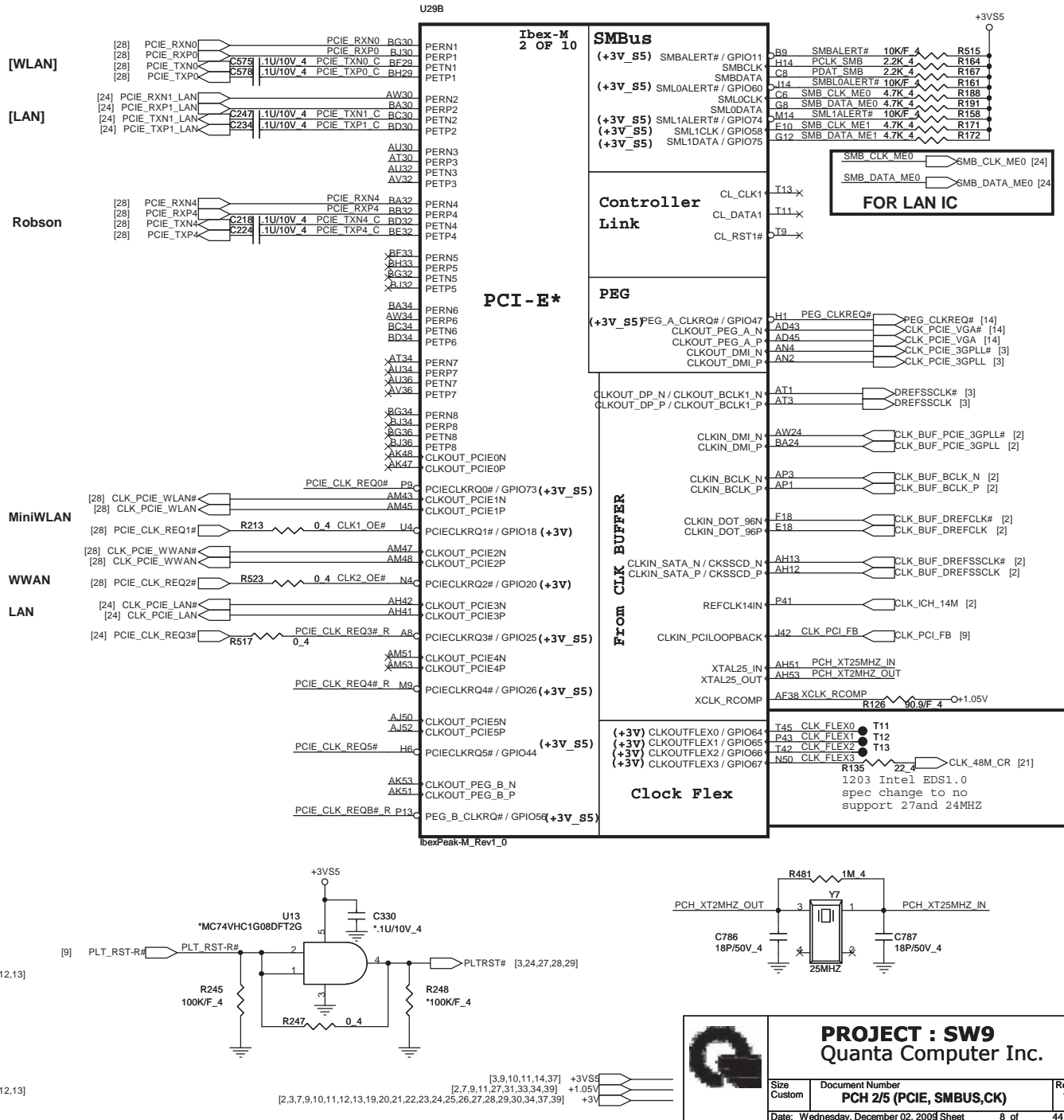
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A
Date:	Wednesday, December 02, 2009 Sheet	7 of 44

IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

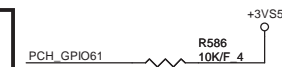
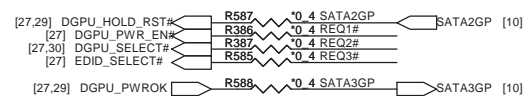


PROJECT : SW9
Quanta Computer Inc.

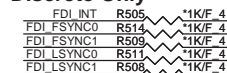
Size	Document Number	Rev
Custom	PCH 2/5 (PCI-E, SMBUS, CLK)	1A

Date: Wednesday, December 02, 2009 Sheet 8 of 44

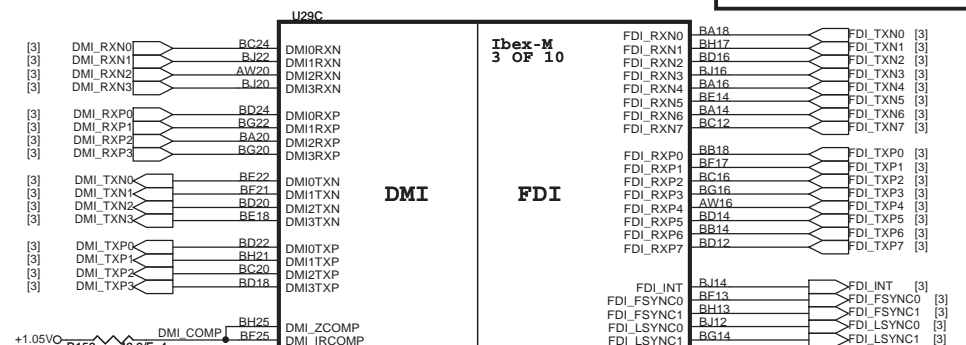
For Switchable only



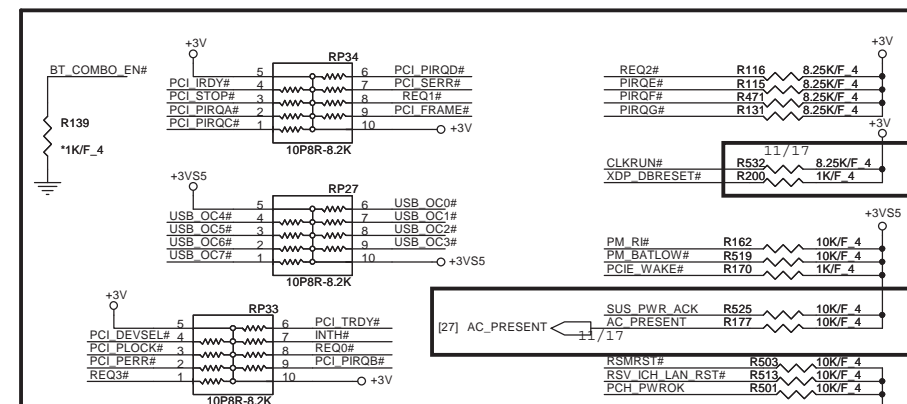
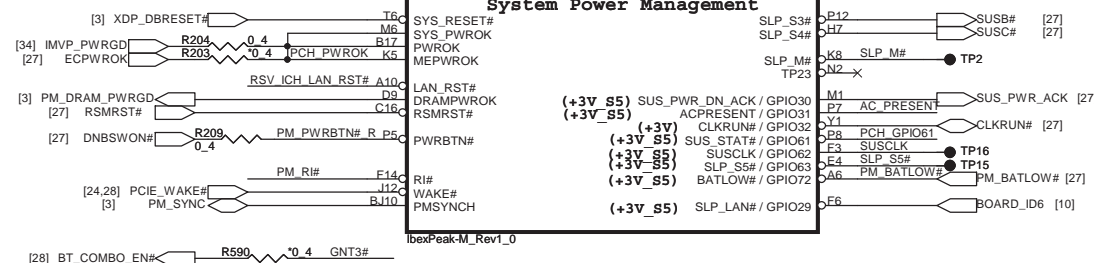
Discrete Only



IBEX PEAK-M (DMI,FDI,GPIO)

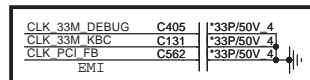
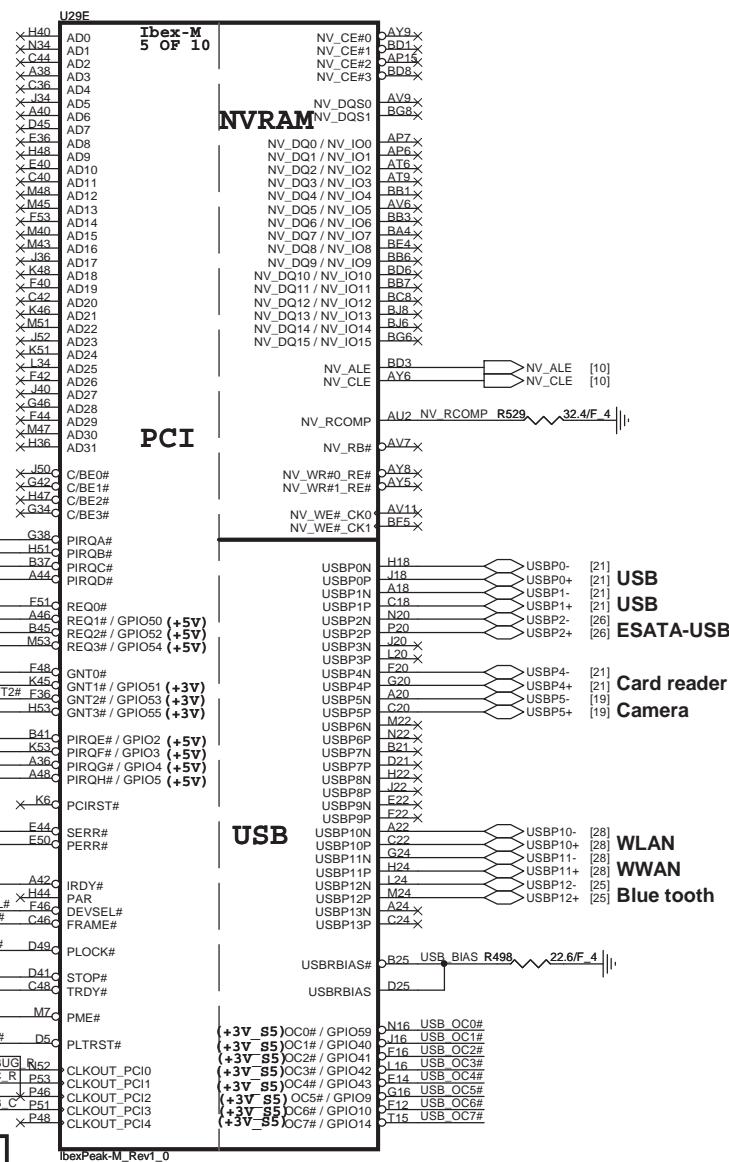
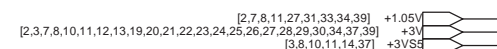


System Power Management



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number PCH 3/5(PCI,ONFI,USB,DMI)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 9 of 44		

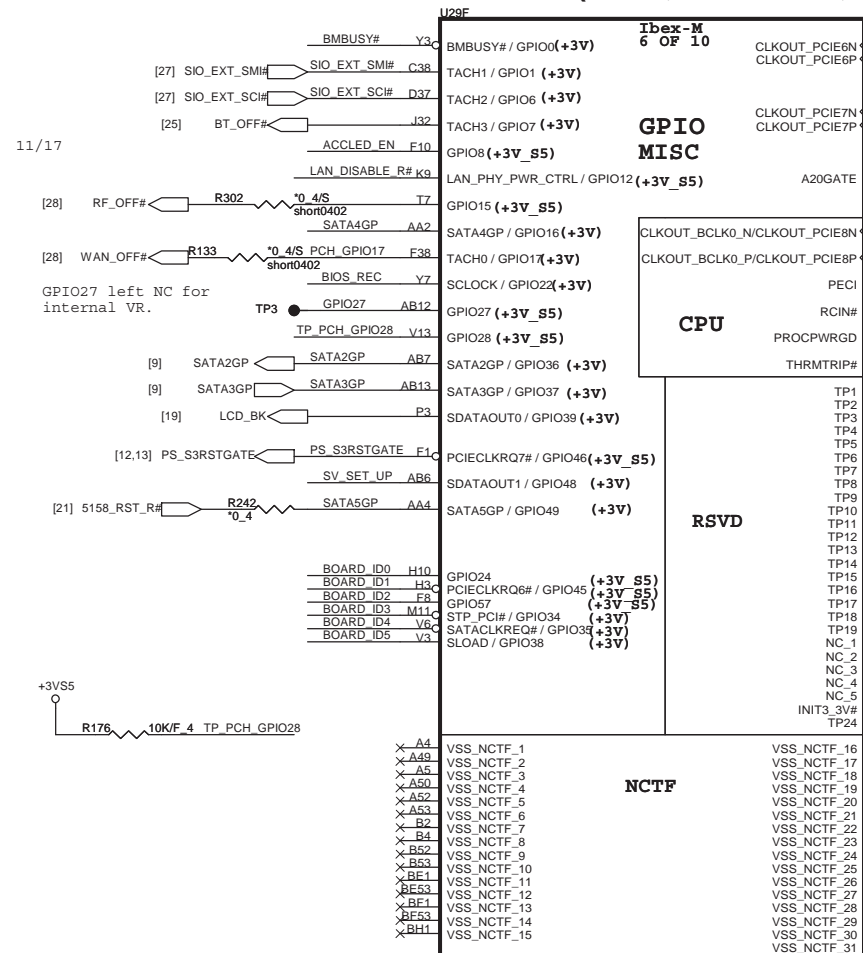


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

<http://hobi-elektronika.net>

IBEX PEAK-M (GND)

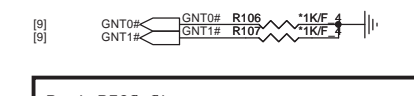
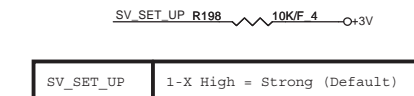
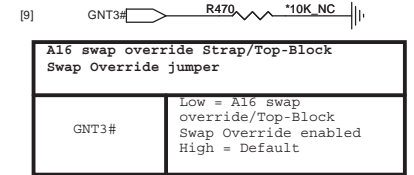
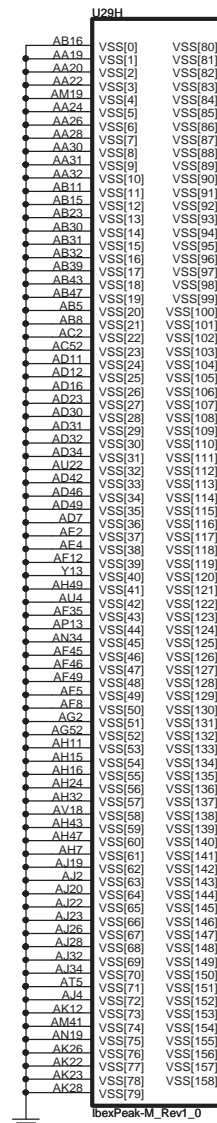
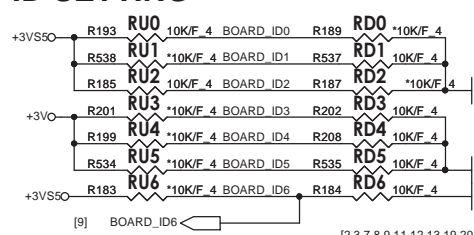
10



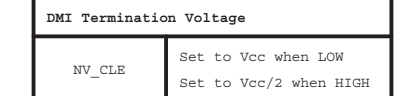
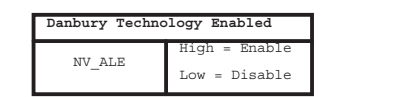
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6" / 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

BOARD ID SETTING



PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

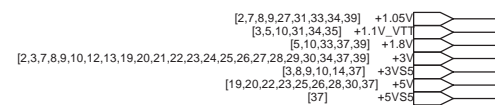
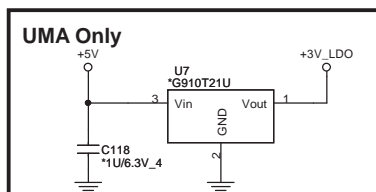
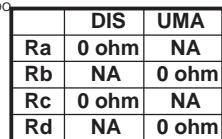


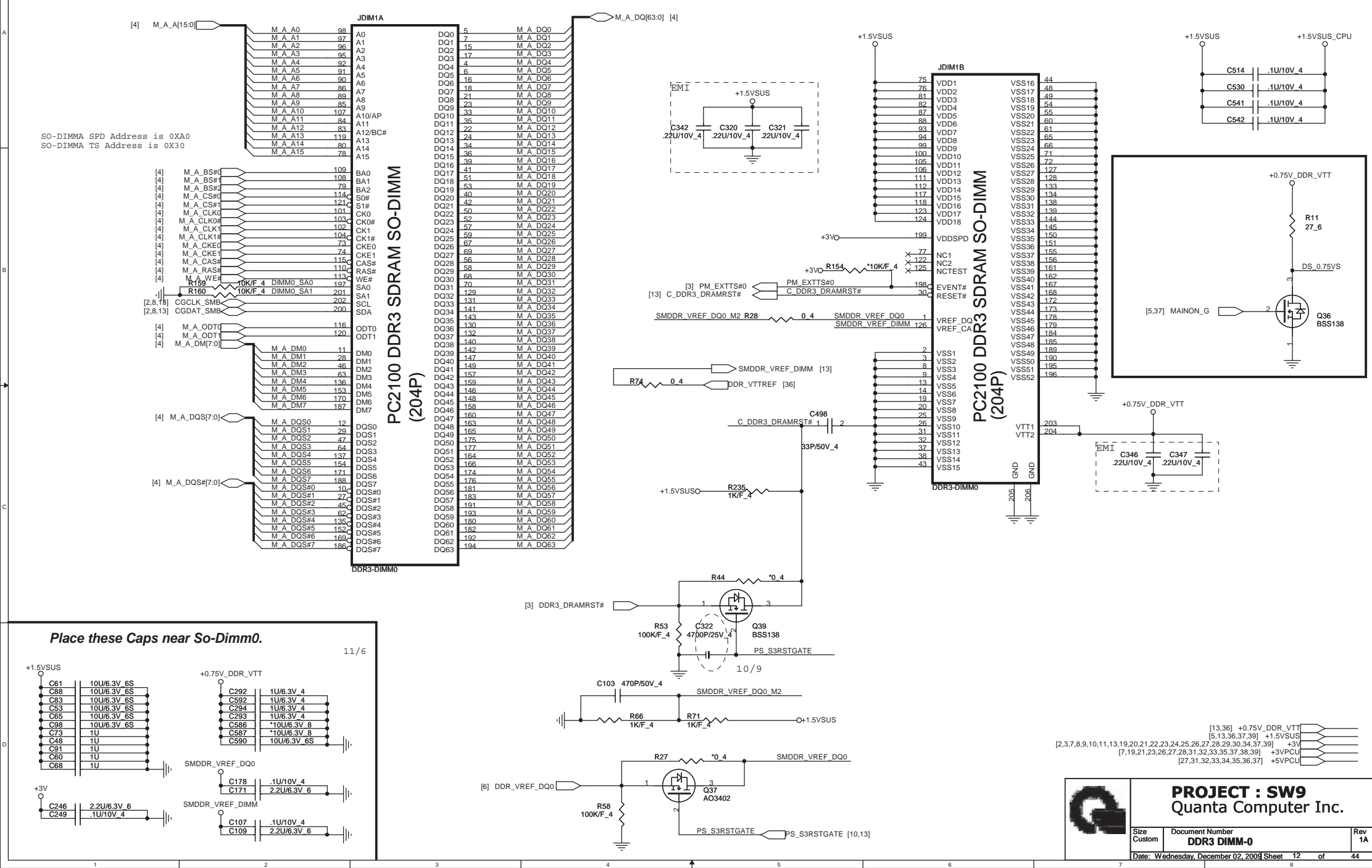
No Reboot Strap

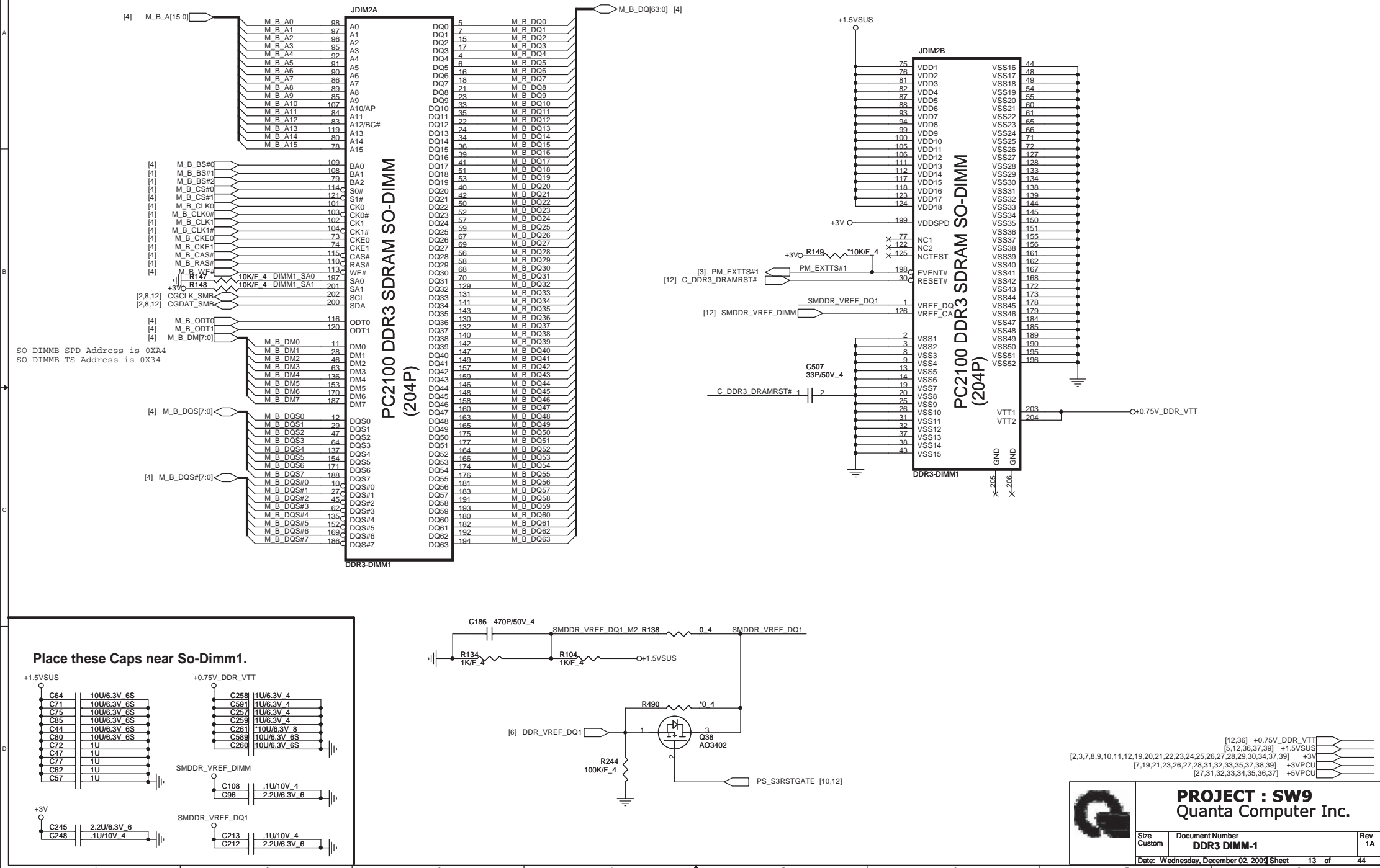


PROJECT : SW9
Quanta Computer Inc.

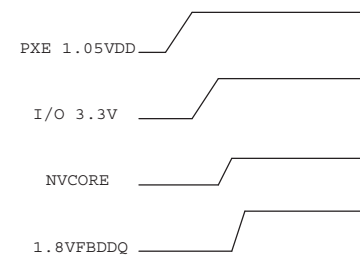
Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	1A
Date:	Wednesday, December 02, 2009 Sheet	10of 44



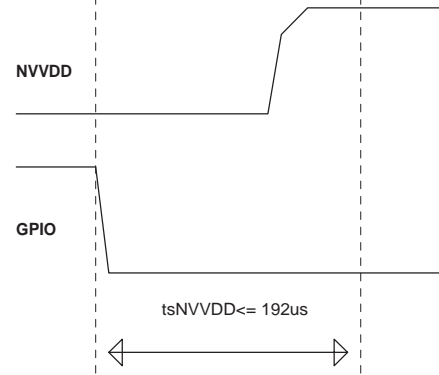




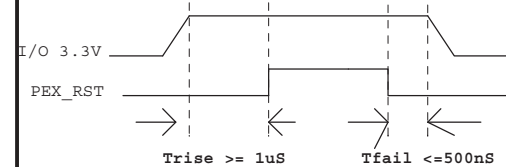
power up sequence



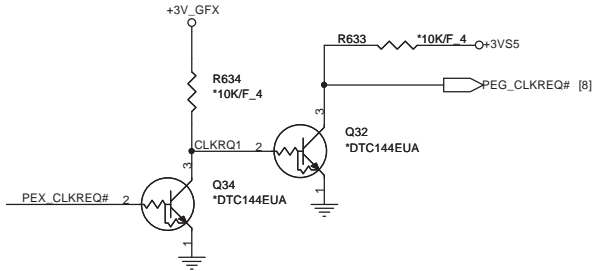
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



For Switchable only

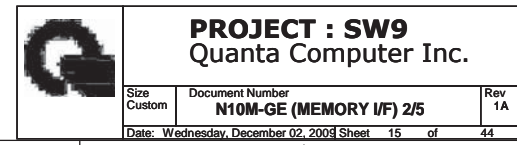


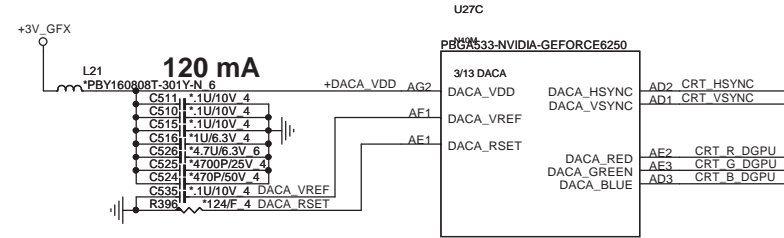
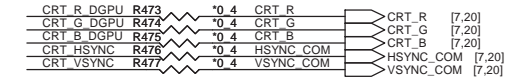
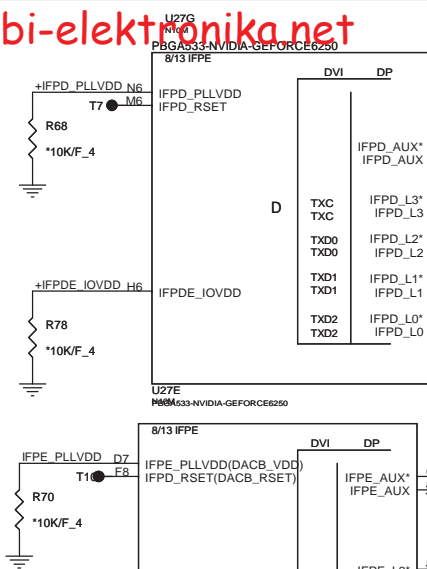
VGA Thermal Circuit ==> Del 6/16




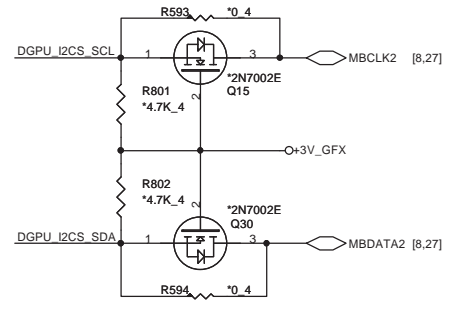
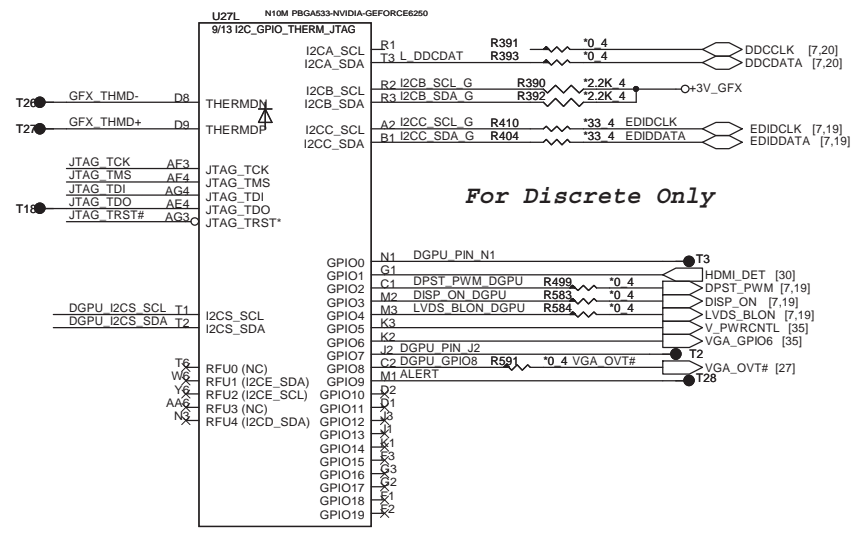
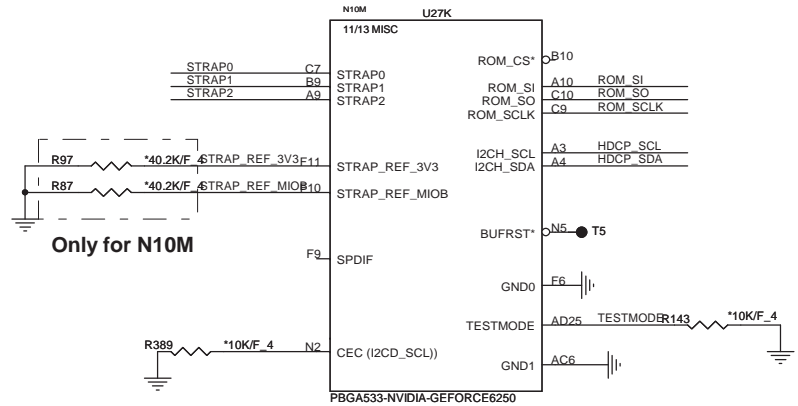
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (PCIE V/F) 1/5	1A
Date: Wednesday, December 02, 2009 Sheet 14 of 44		





	<h1>PROJECT : SW9</h1> <h2>Quanta Computer Inc.</h2>		
	Size Custom	Document Number	Rev 1A
	<h3>N10M-GE (DISPLAY) 3/5</h3>		
Date: Wednesday, December 02, 2009 Sheet 16 of 44			



CRTP	PCI_DEVID:	STRAP2
N11P-GE1	0x0A29	1001 PU 10K
N11M-GE1	0x0A75	1010 PD 30K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

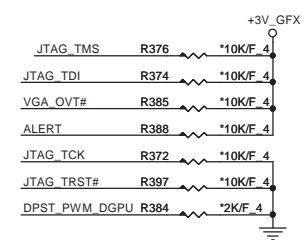
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)] Default: Hynix VRAM

10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

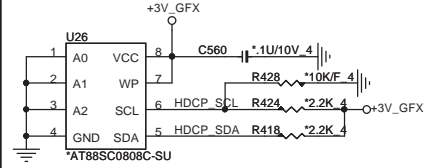
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	IDGH1G-04A1F1C-16X	PD 10K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	H5TQ1G63BFR-12C	PD 15K
0101		Reserved		
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	PD 20K
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646E-EC12	



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDPC ROM

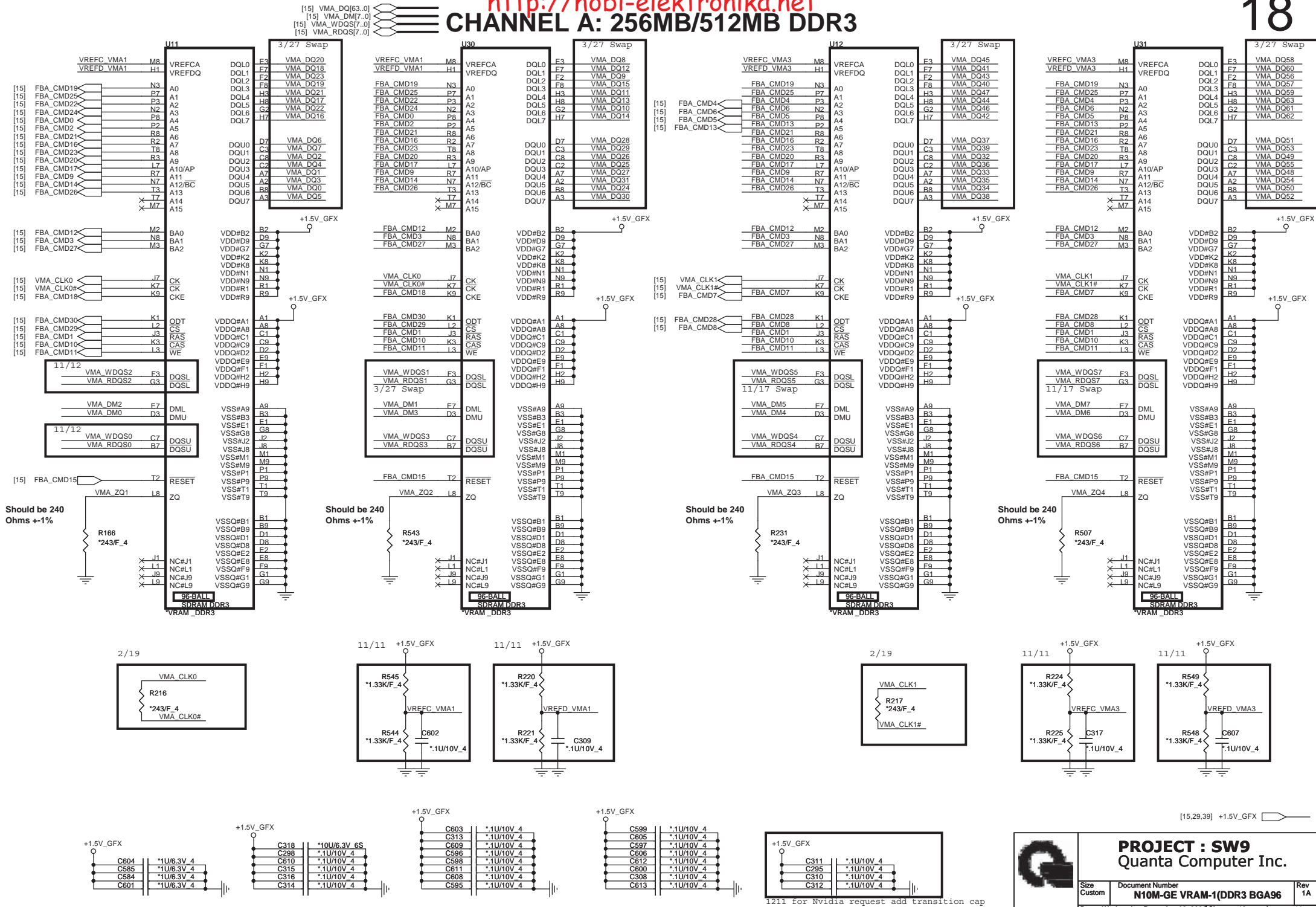


DHCP ROM	
HDPC_SCL	Low: Crypto ROM Hi: I2C ROM



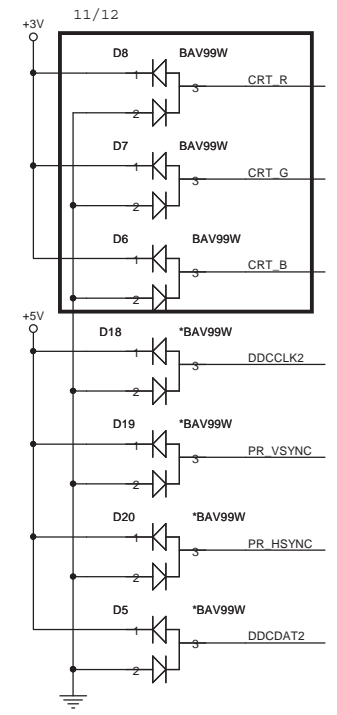
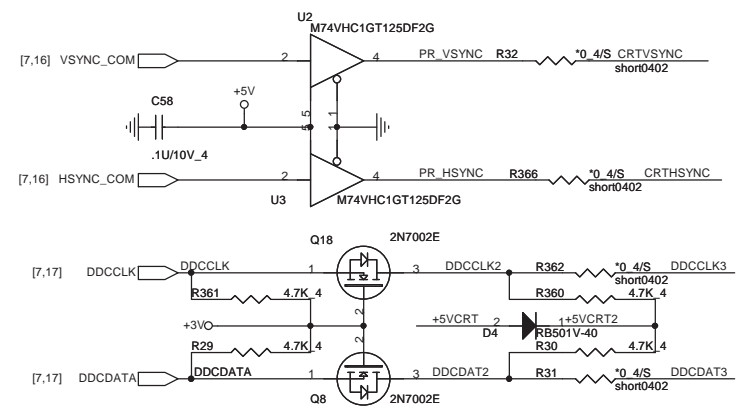
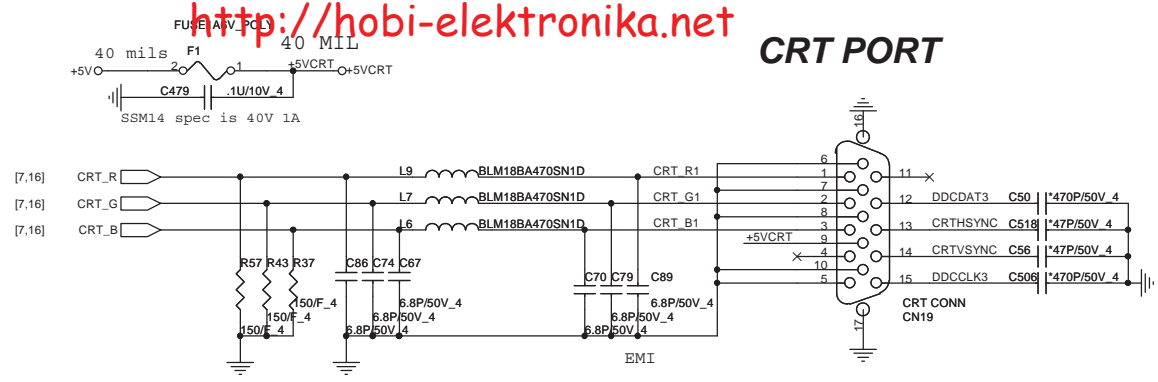
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	1A
Date: Wednesday, December 02, 2009 Sheet 17 of 44		



PROJECT : SW9
Quanta Computer Inc.

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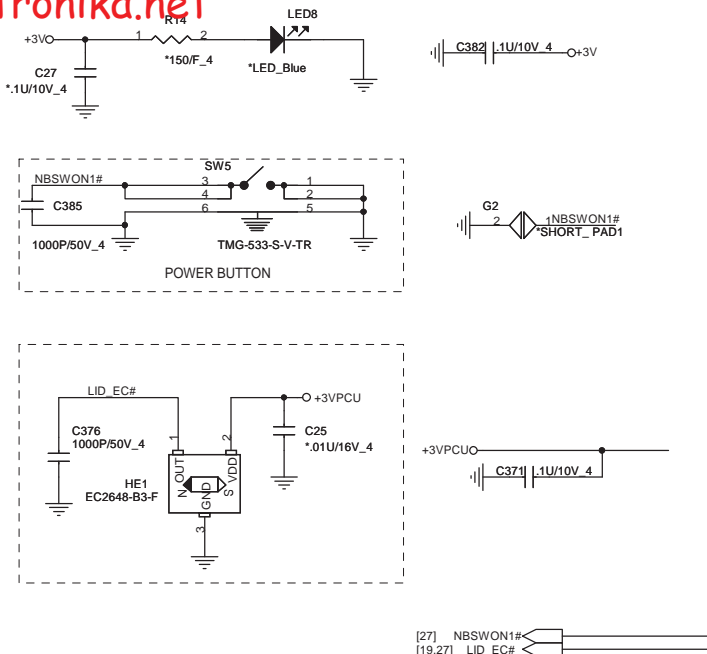
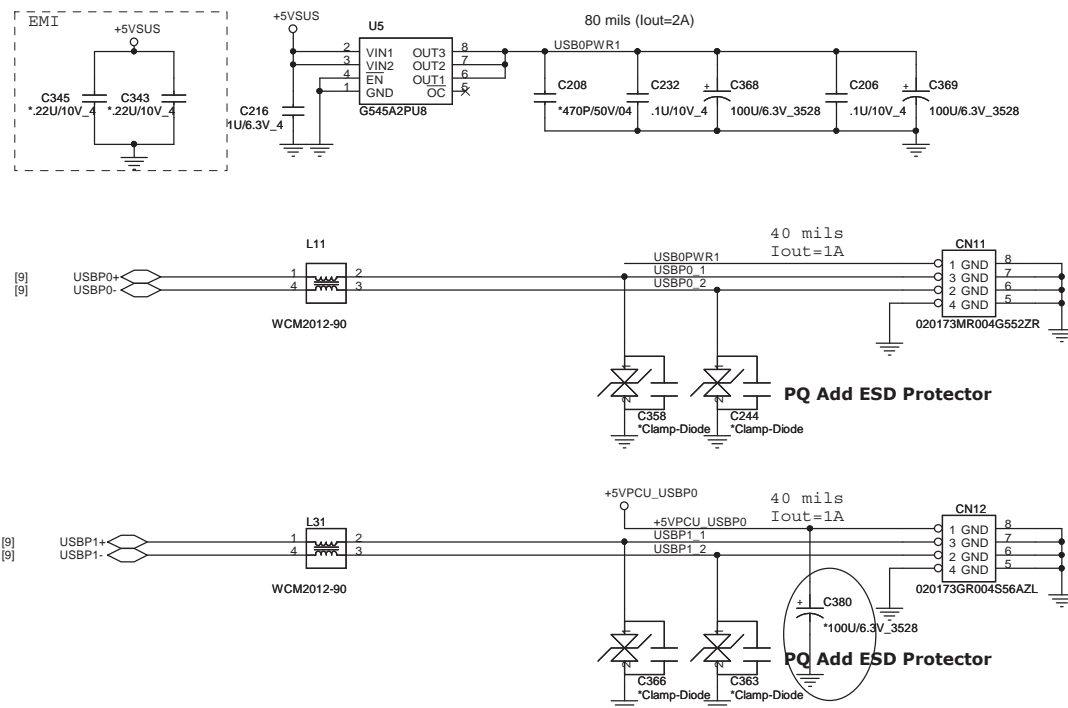
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A
Date: Wednesday, December 02, 2009 Sheet 20 of 44		

USB CONNECTOR

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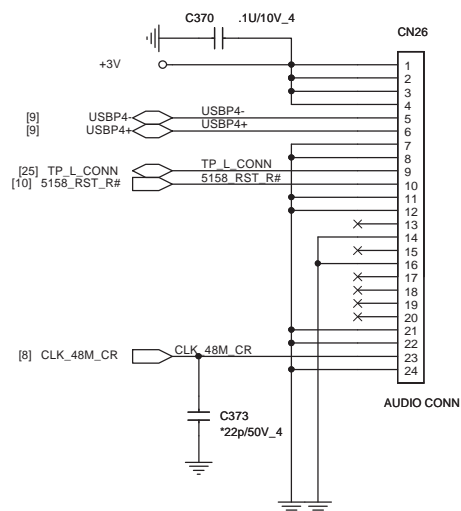
21



1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

TO M/B CON.

PV Change CN2 footprint 88501-2001-24p-I-nb5

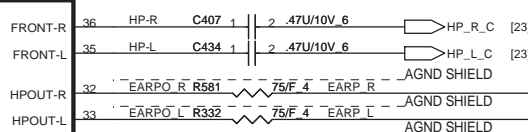
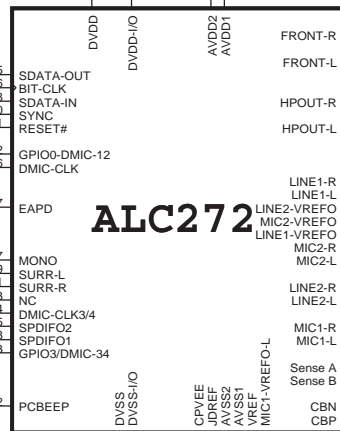
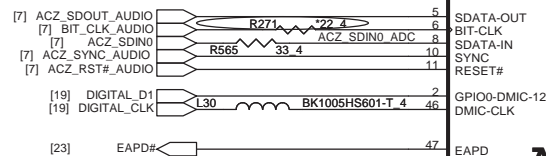
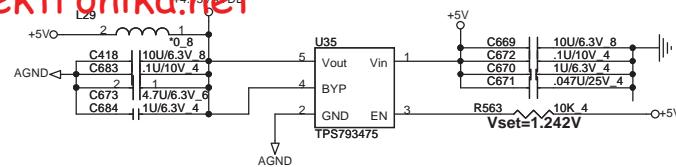
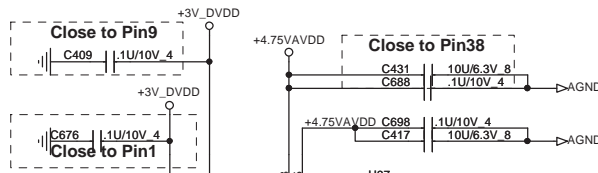
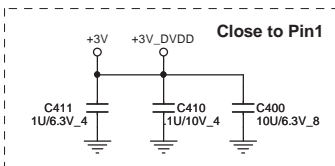


[2,3,7,8,9,10,11,12,13,19,20,22,23,24,25,26,27,28,29,30,34,37,39] +3VPCU +3V

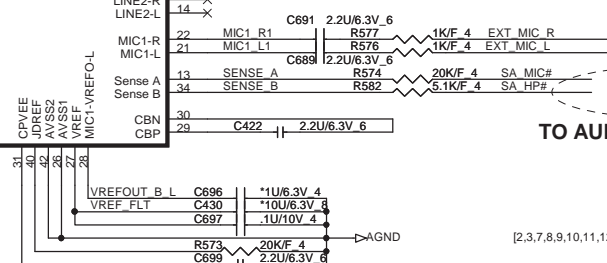
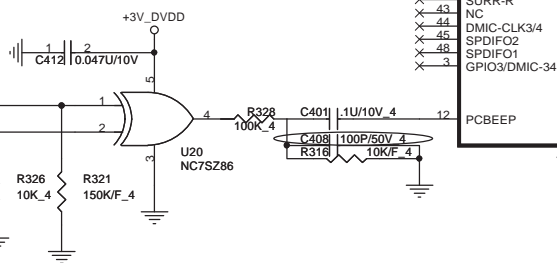
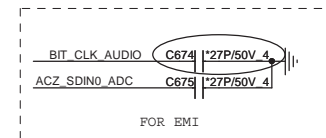


PROJECT : SW9
Quanta Computer Inc.

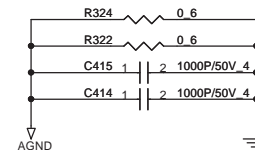
Size	Document Number	Rev
Custom	RTS5159 &CR SOCKET	1A
Date:	Wednesday, December 02, 2009	Sheet 21 of 44



To Internal Speakers

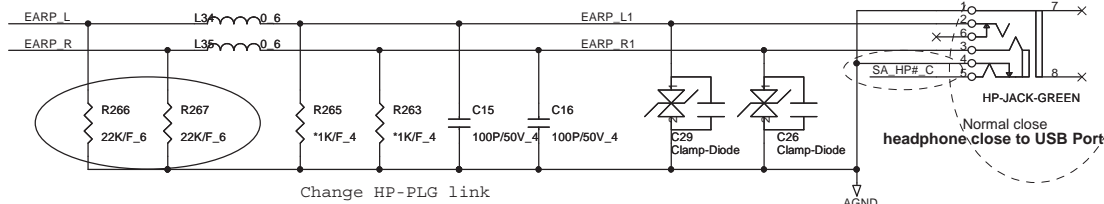


TO AUDIO/B CON.

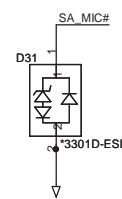
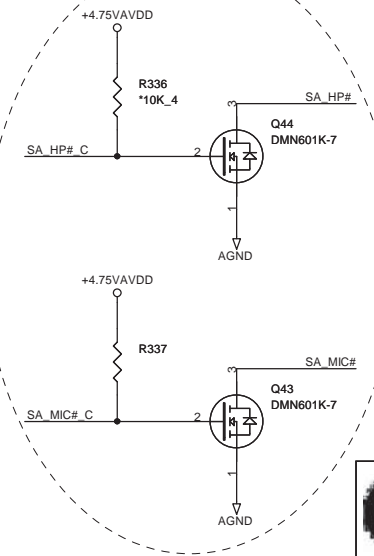
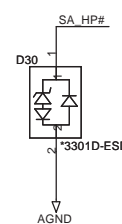
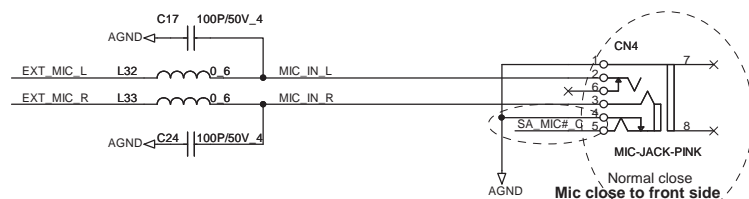


AUDIO CONNECTOR

10/07



AUDIO JACKS CHANGE TO NORMAL OPEN



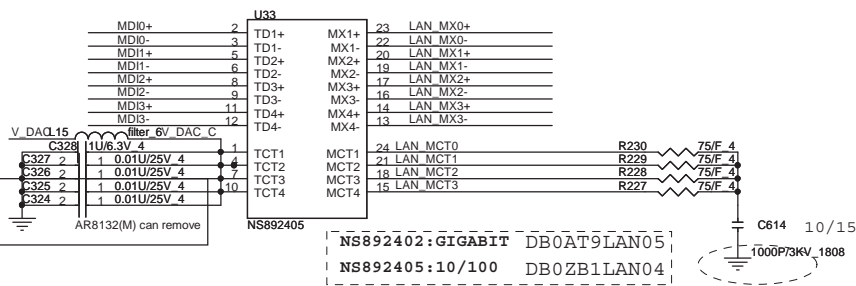
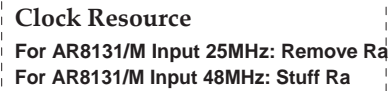
PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Azalia ALC272/BT CONN		
Date: Wednesday, December 02, 2009		Sheet 22 of 44

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

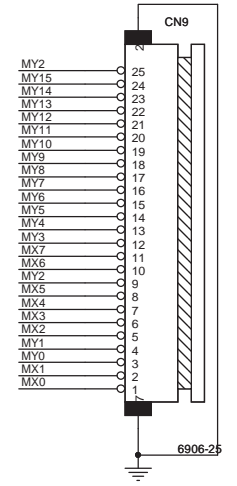
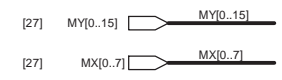
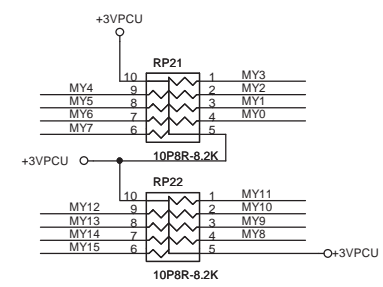
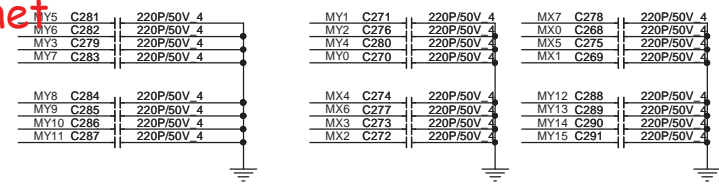
Close to U21 For EMI

Size Custom	Document Number AMP_TPA6017/SPK/MDC/LED	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 23 of 44		

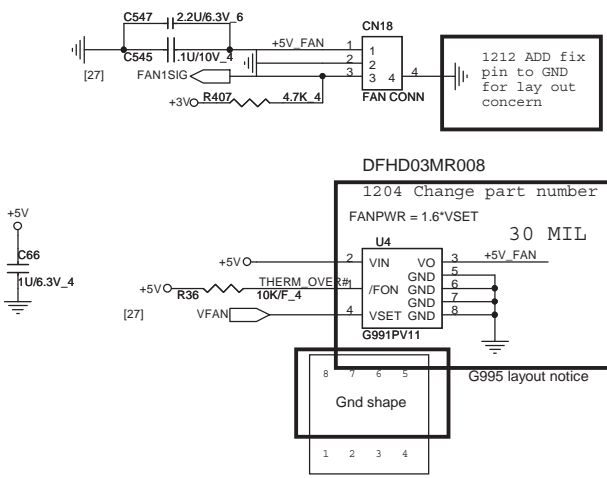


Size Custom	Document Number AR8131(M)/RJ45	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 24 of 44		

KEYBOARD CON.

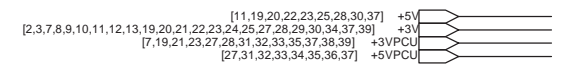
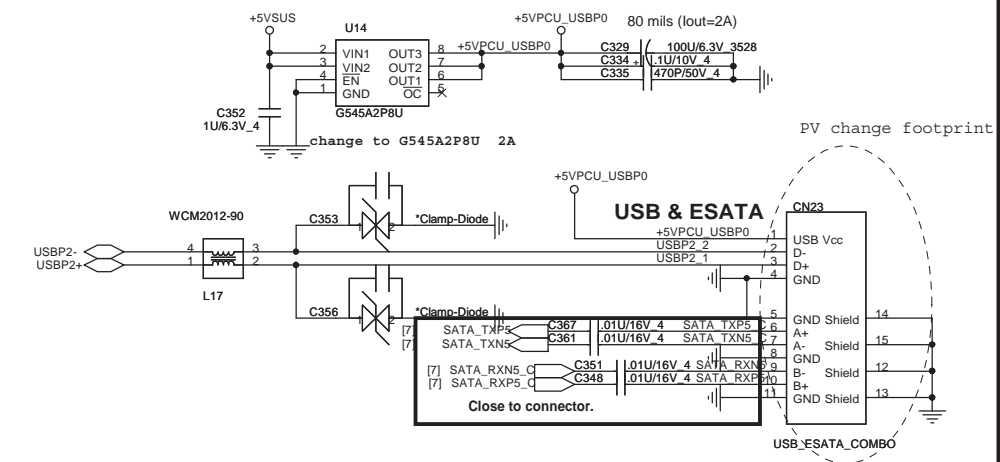


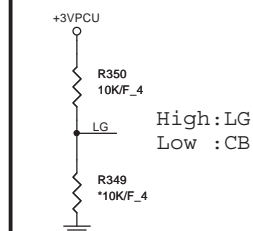
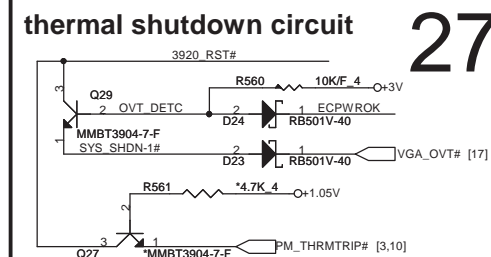
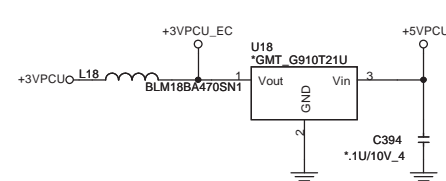
CPU FAN



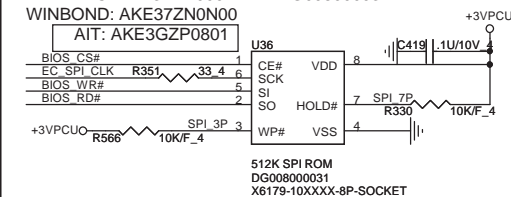
Capacity board Con.

E-SATA/USB COMBO

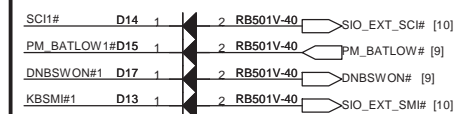
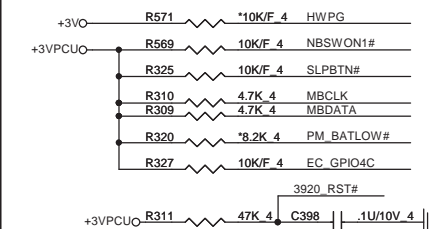




512K byte SPI ROM for EC	SPI ROM Socket
MXIC: AKE3KZP0001	DG0080000031

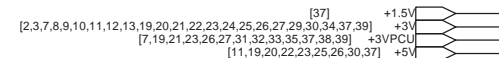


ID	Ra	Rb
120W	10K	N/A
65W/90W	N/A	10K



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number KB3926/ROM/TP	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 27 of 44		

WLAN

PROJECT : SW9
Quanta Computer Inc.

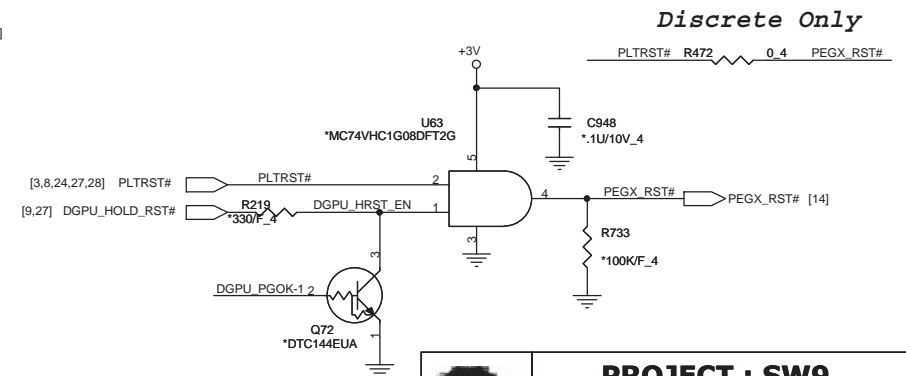
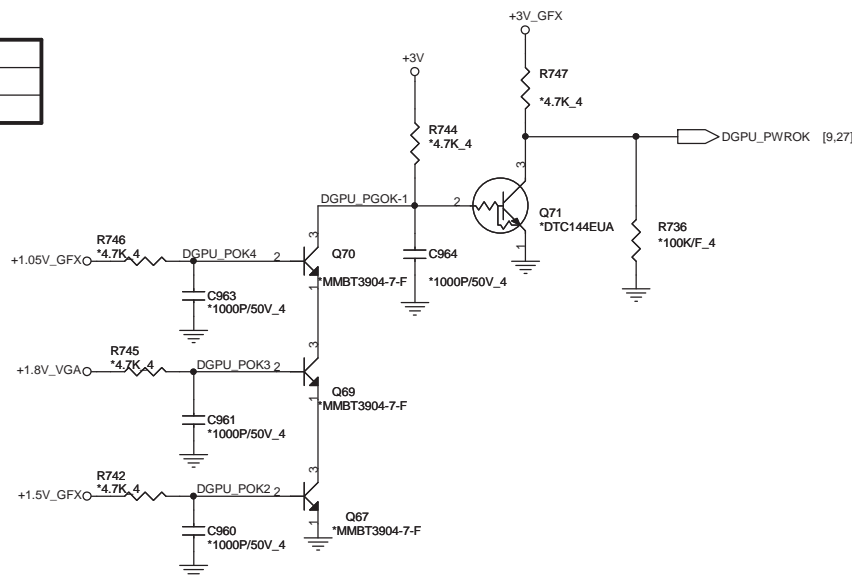
Size Custom	Document Number MINI PCIE CONN X2	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 28 of 44		

DEL Switch IC

DEL Switch IC

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

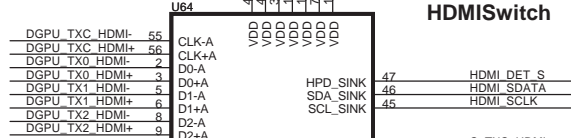
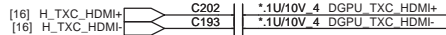
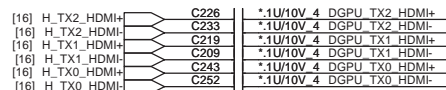
SELx	Ay
LOW	B1
HIGH	B2



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number LVDS / CRT Switch	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 29 of 44		

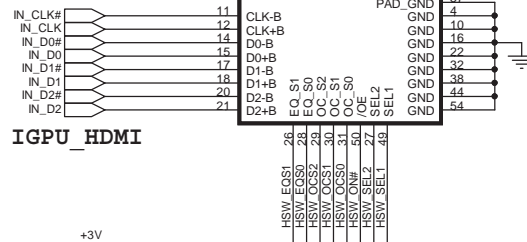
DGPU_HDMI



HDMISwitch



IGPU_HDMI



To HDMI Conn.

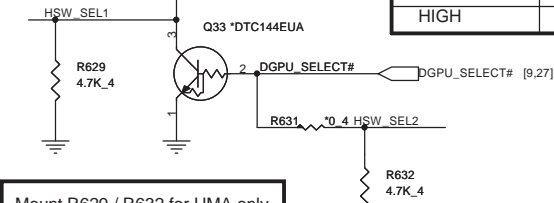
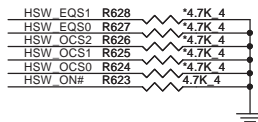
SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

OC SETTING

S2 S1 S0 = 1 : 1 : 1 500mV 0dB Default
 S2 S1 S0 = 1 : 1 : 0 750mV 0dB
 S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
 S2 S1 S0 = 1 : 0 : 0 600mV 0dB
 S2 S1 S0 = 0 : 1 : 1 500mV 0dB
 S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
 S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
 S2 S1 S0 = 0 : 0 : 0 500mV 6dB

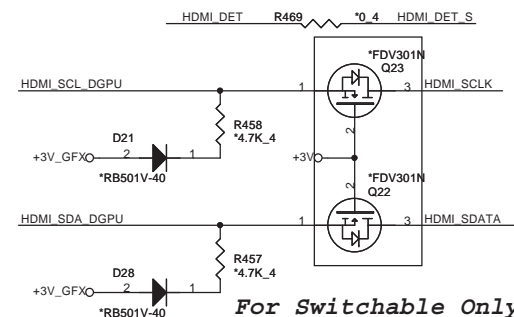
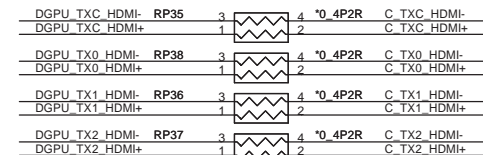
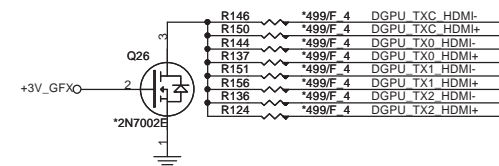
EQ SETTING

S1 S0 = 1 : 1 3dB Default
 S1 S0 = 1 : 0 8dB
 S1 S0 = 0 : 1 3dB
 S1 S0 = 0 : 0 15dB



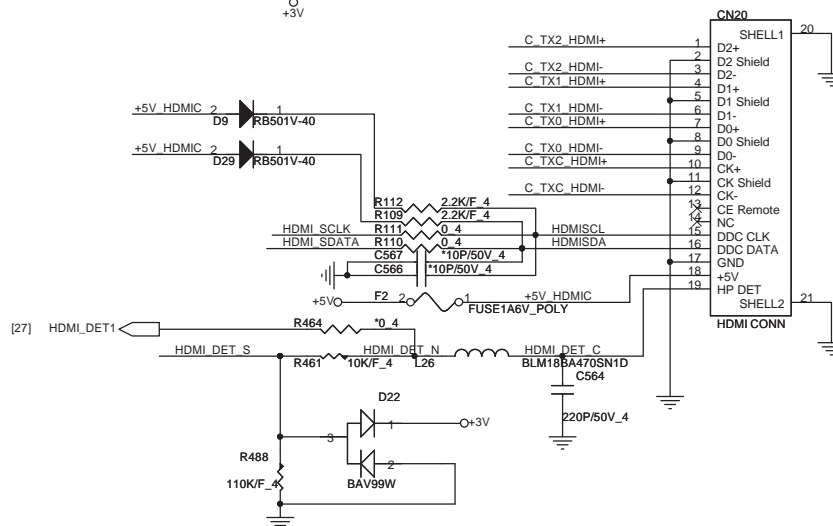
Mount R629 / R632 for UMA only

Only for NVIDIA

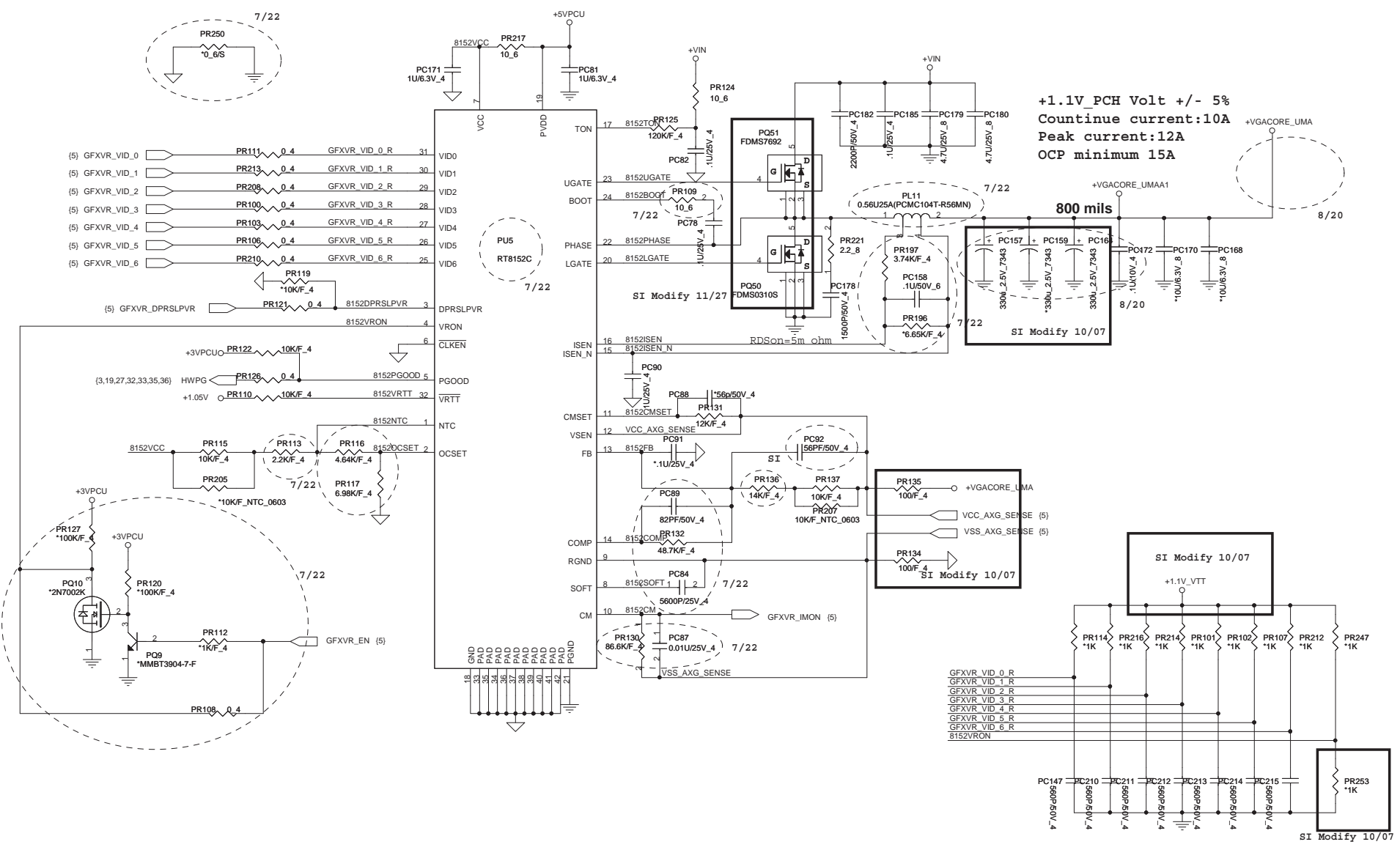


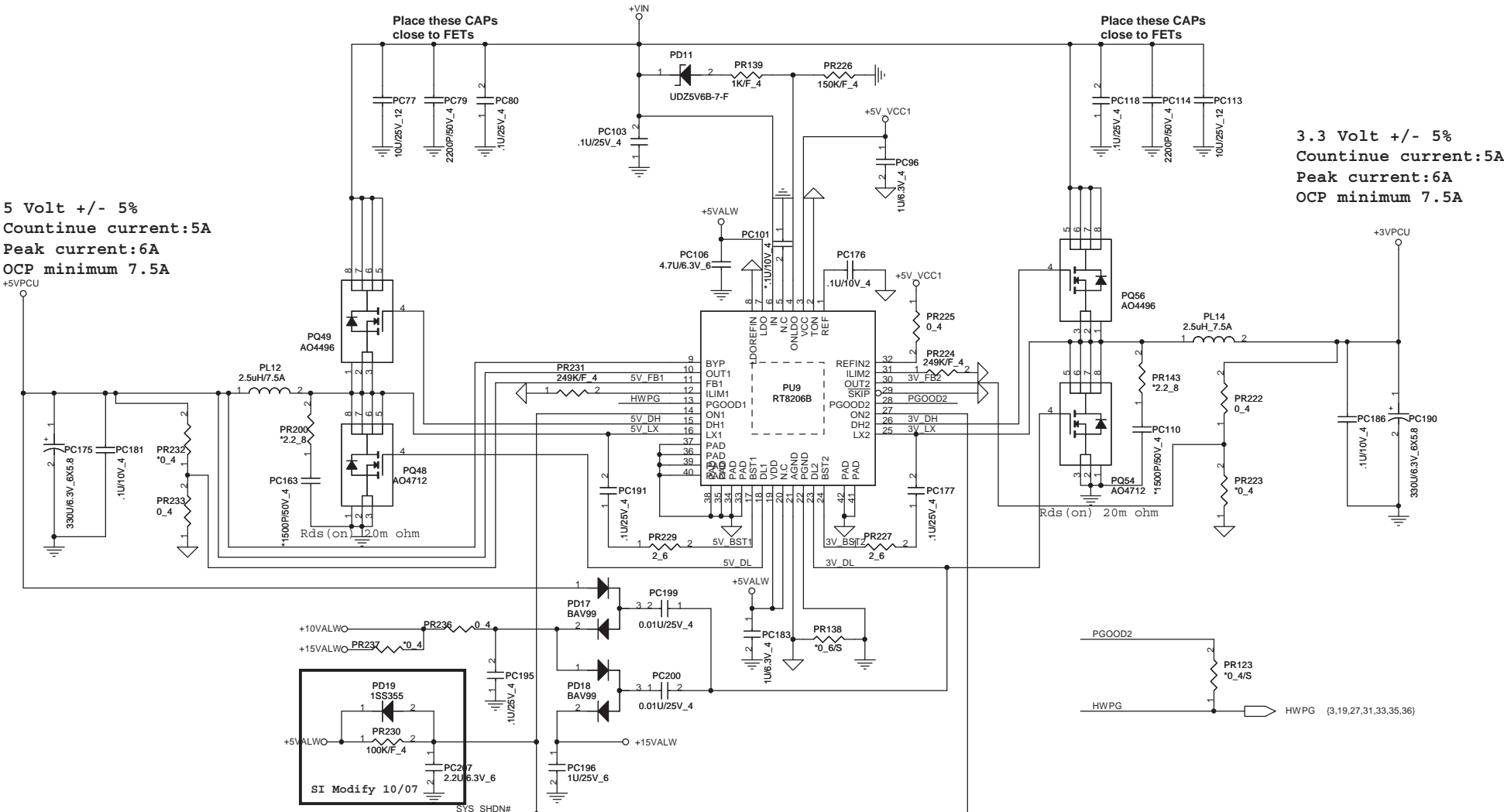
For Switchable Only

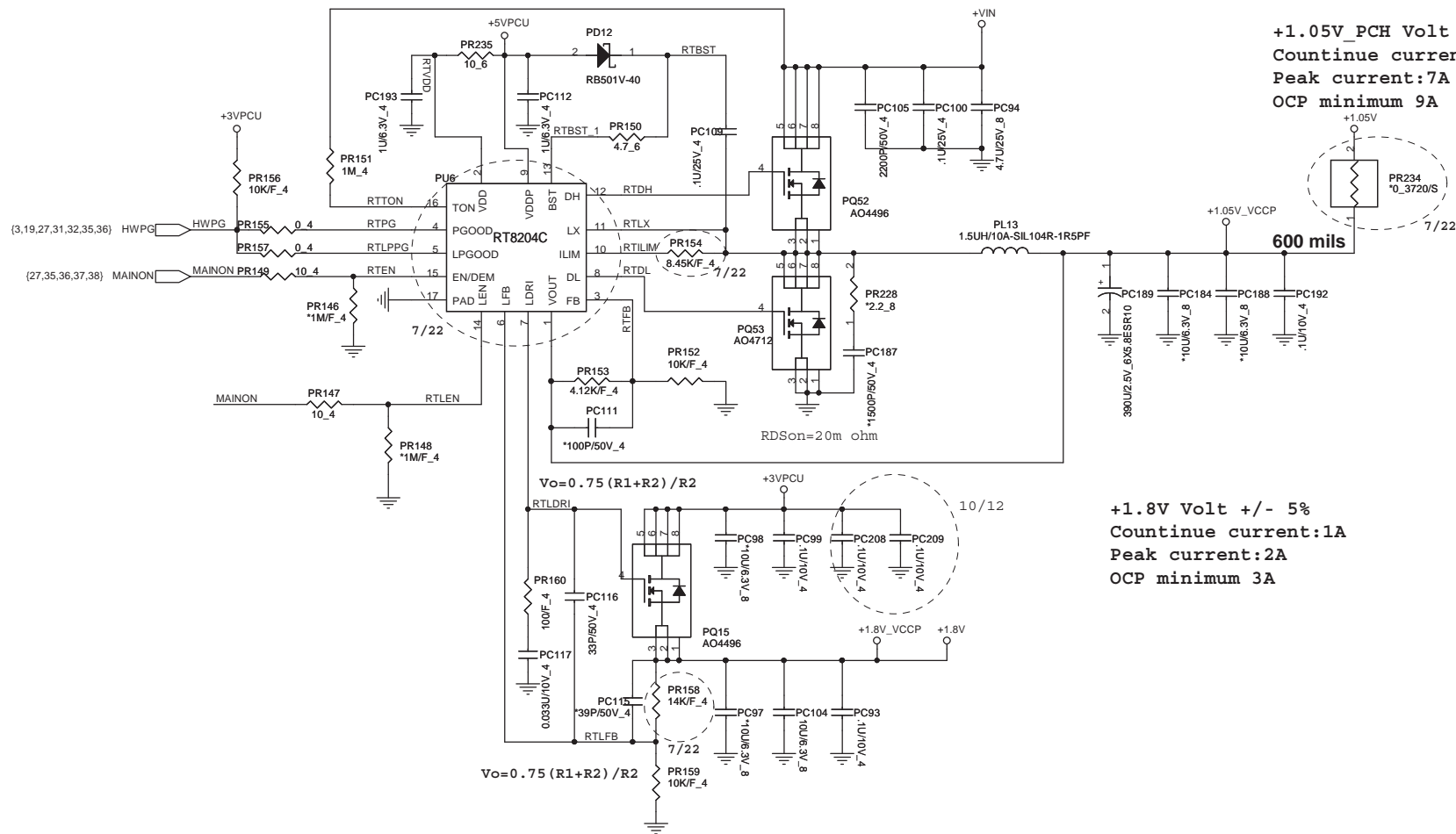
HDMI PORT



PROJECT : SW9
 Quanta Computer Inc.

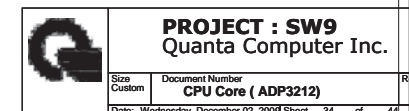




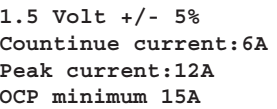


PROJECT : SW9
Quanta Computer Inc.

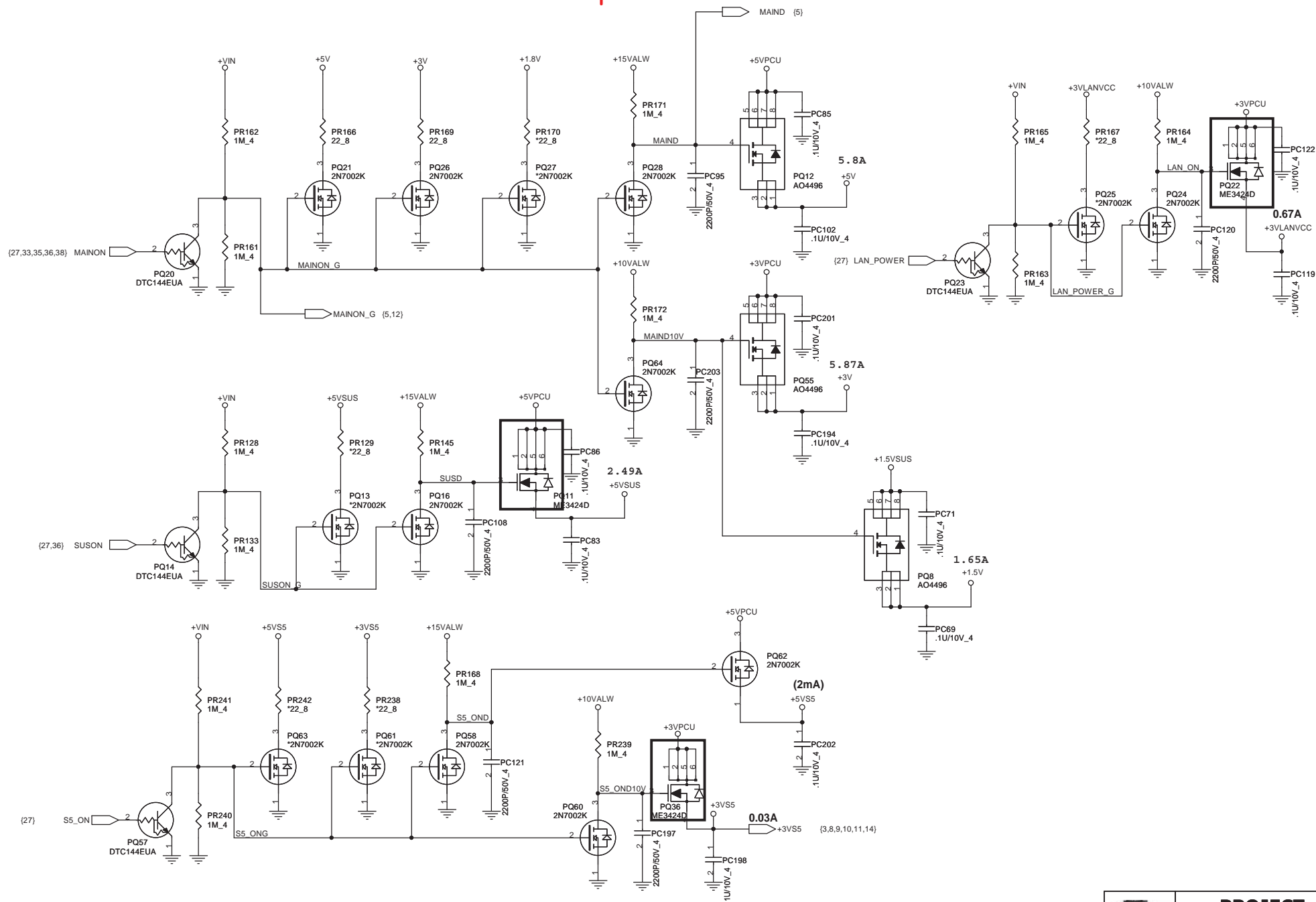
Size	Document Number	Rev
Custom	PCH +1.05V (RT8204)	1A
Date: Wednesday, December 02, 2003 Sheet 33 of 44		



OCF Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm



Size Custom	Document Number DDR3 (RT8207)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 36 of 44		



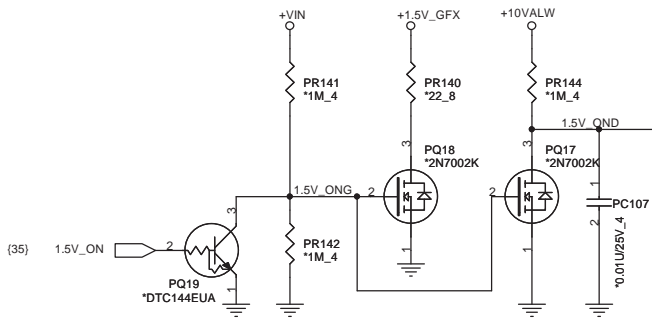
PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 1A
Date: Wednesday, December 02, 2003 Sheet 37 of 44		



Size Custom	Document Number Charger (ISL6251)	Rev 1A
Date: Wednesday, December 02, 2008 Sheet 38 of 44		

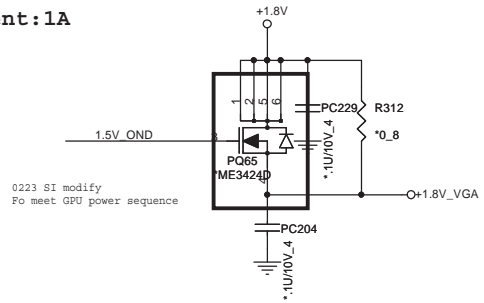
For Discrete or switchable Only



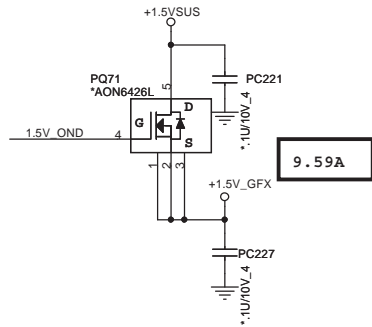
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only

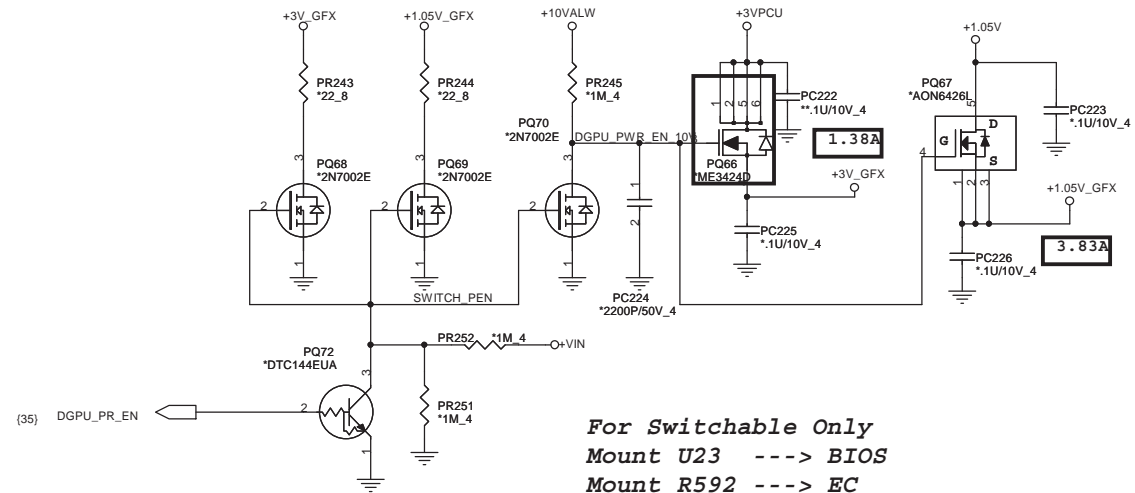
+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A



0223 SI modify
Fo meet GPU power sequence



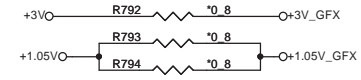
9.59A



For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC

R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



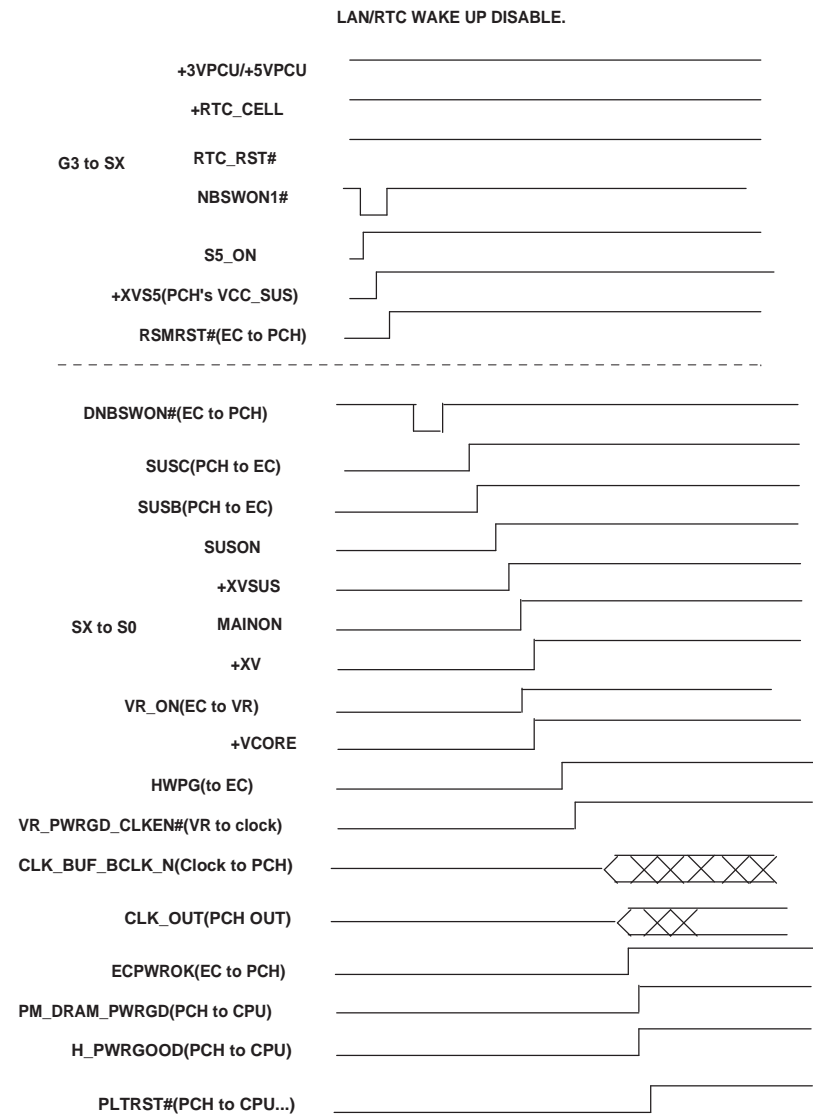
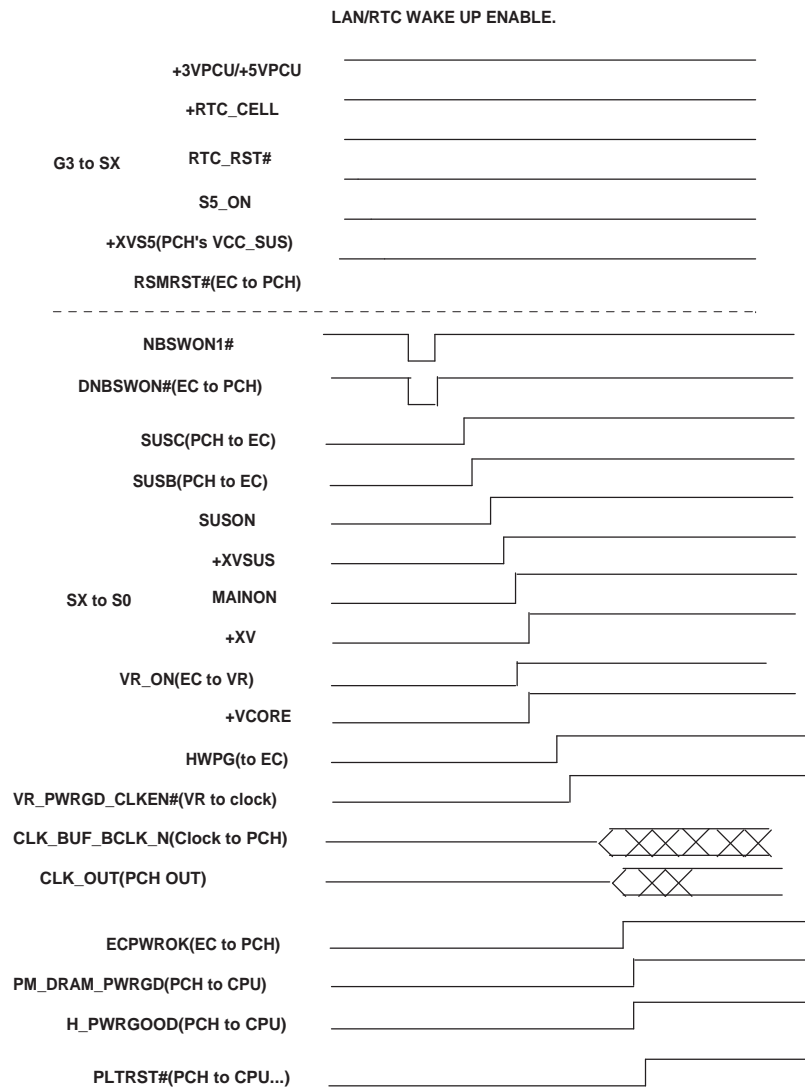
- For Hybrid DGPU Power Rails Sequence**
1. +3V_GFX, +1.05V_GFX
 2. +VGA_CORE -> DGPU_PG
 3. 1.5V_GFX, +1.8V_GFX



PROJECT : SW9
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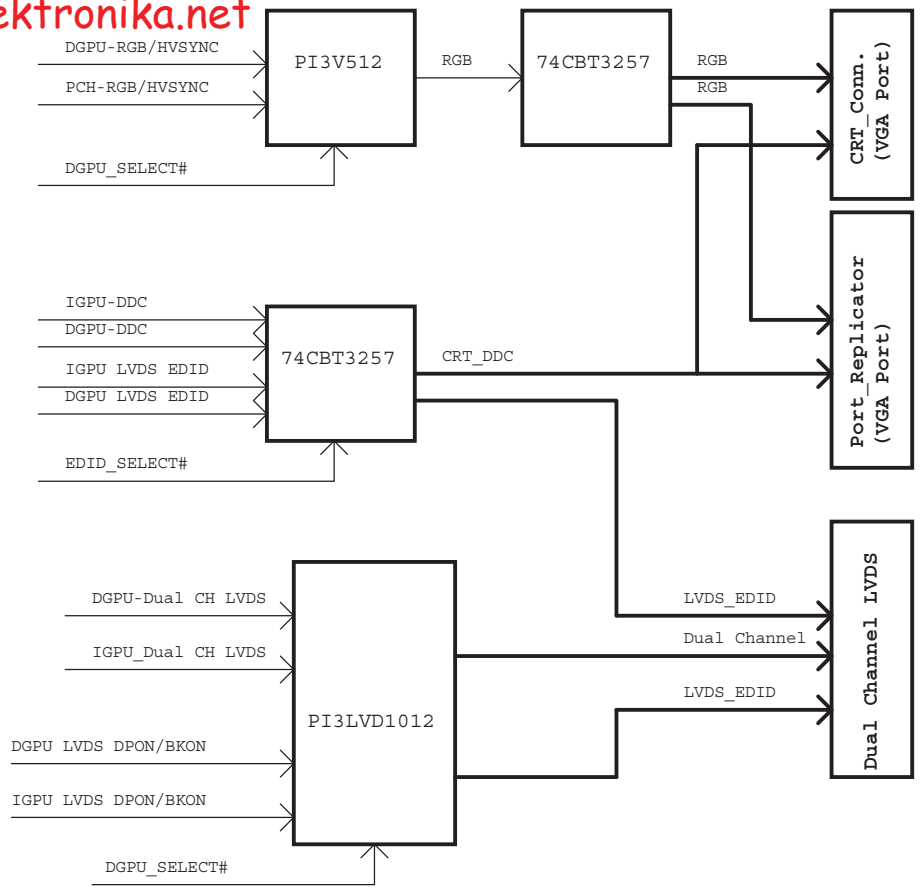
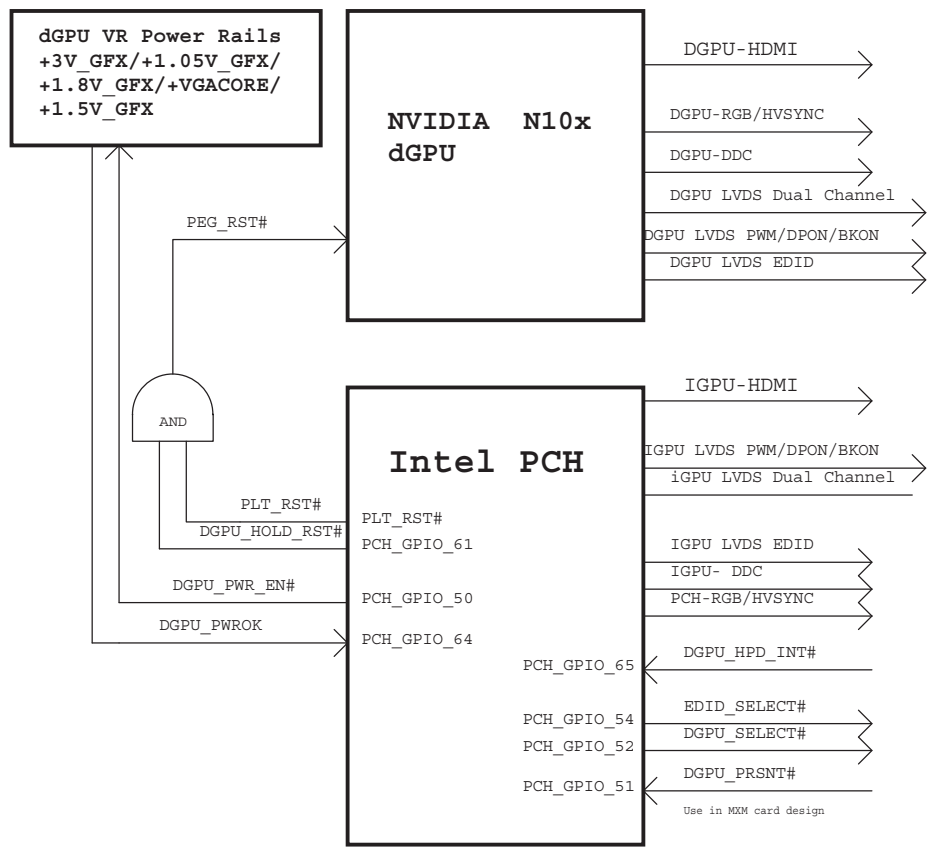
Size A3	Document Number Switchable Power	Rev 1A
Date: Wednesday, December 02, 2009	Sheet 39 of 44	

Power up sequence



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number Power up sequence	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 40 of 44		



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSENT#
PCH_GPIO53	PWM_SELECT#

